

# **Tema 12.2 - Manejo básico EDK. Creación de un Periférico GPIO**

Sistemas Electrónicos para Automatización  
Grado en Ingeniería Electrónica, Robótica y  
Mecatrónica

Hipólito Guzmán Miranda

## Contenido

- Adición del BSP de la LX9 a EDK
- Creación del proyecto de EDK
- Secciones importantes de EDK
- Creación de un periférico GPIO

## Contenido

- Adición del BSP de la LX9 a EDK
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## Adición del Board Support Package de la LX9 Microboard

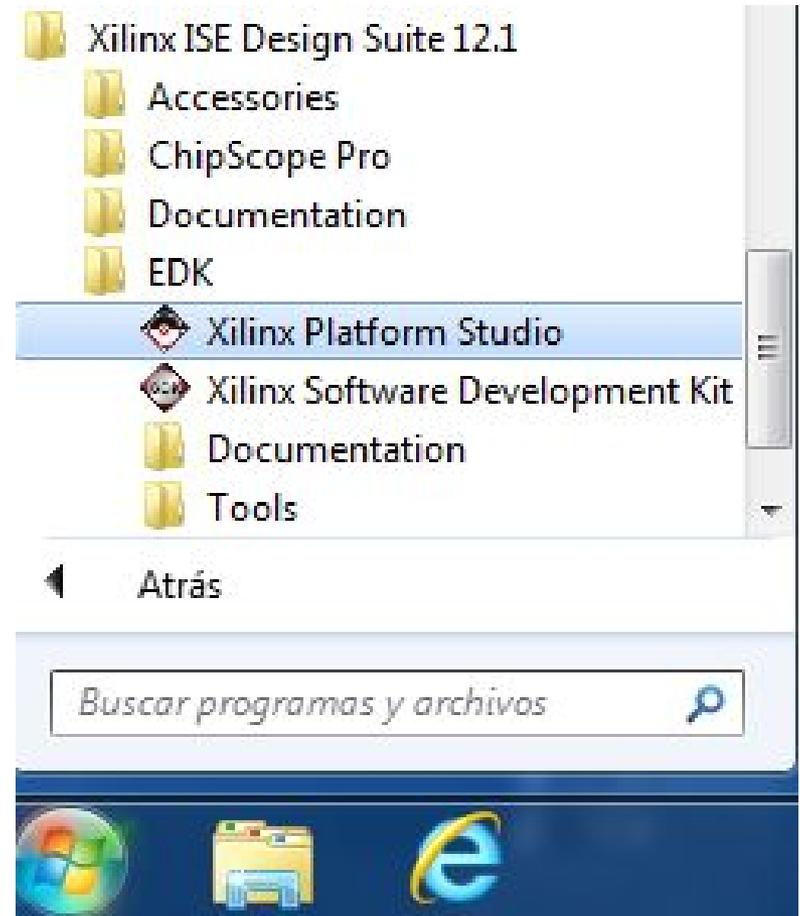
- Descargar el paquete de recursos `avnet_edk12_4_xbd_files.zip` de la página de la asignatura
- Descomprimir y copiar los ficheros extraídos a `<EDK>\board\`, donde EDK es la carpeta donde está instalado EDK.
- Tras la copia debe haber una carpeta `<EDK>\board\Avnet` en la que se encuentren los ficheros de las tarjetas de Avnet, en particular los de la LX9 microboard (la que utilizaremos en la asignatura)

## Contenido

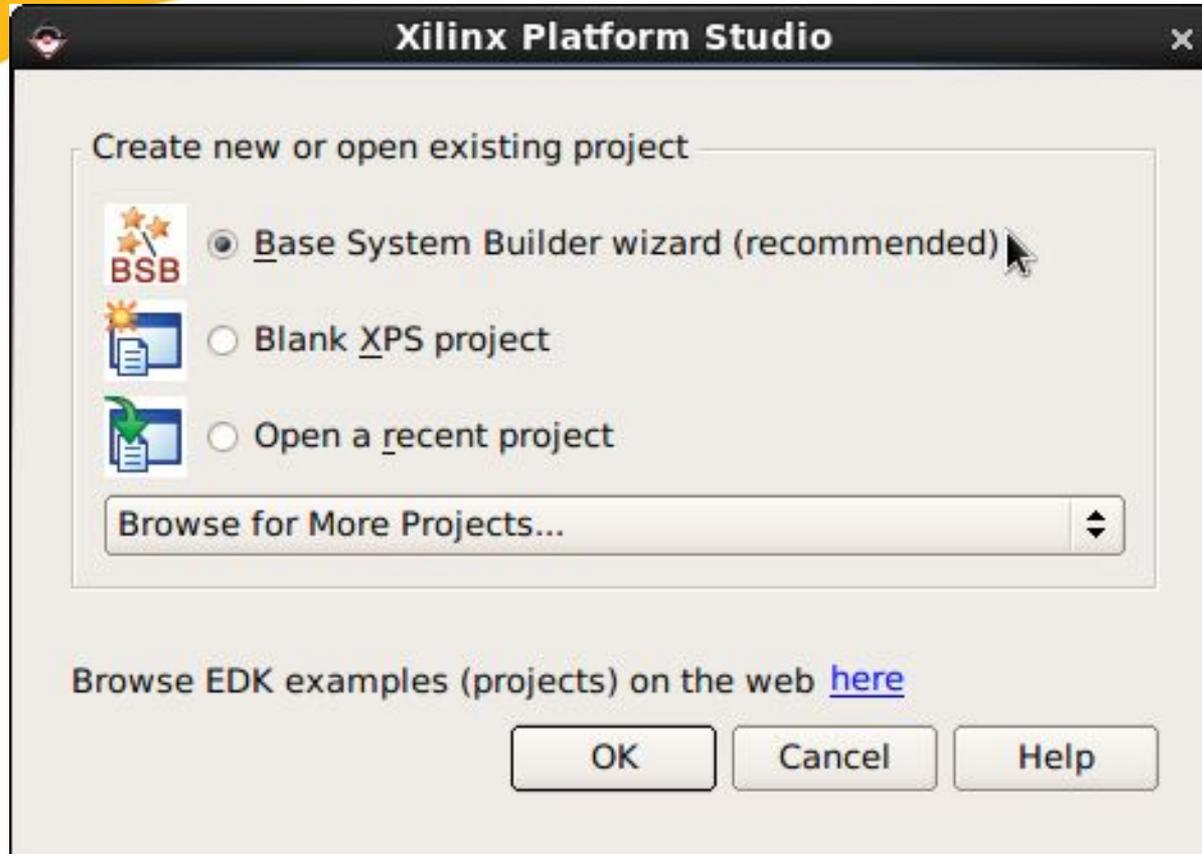
- Adición del BSP de la LX9 a EDK
- **Creación del proyecto de EDK**
- Secciones importantes de EDK
- Creación de un periférico GPIO

# Creación del proyecto EDK

Arrancamos  
Xilinx Platform Studio  
(XPS) 12.1

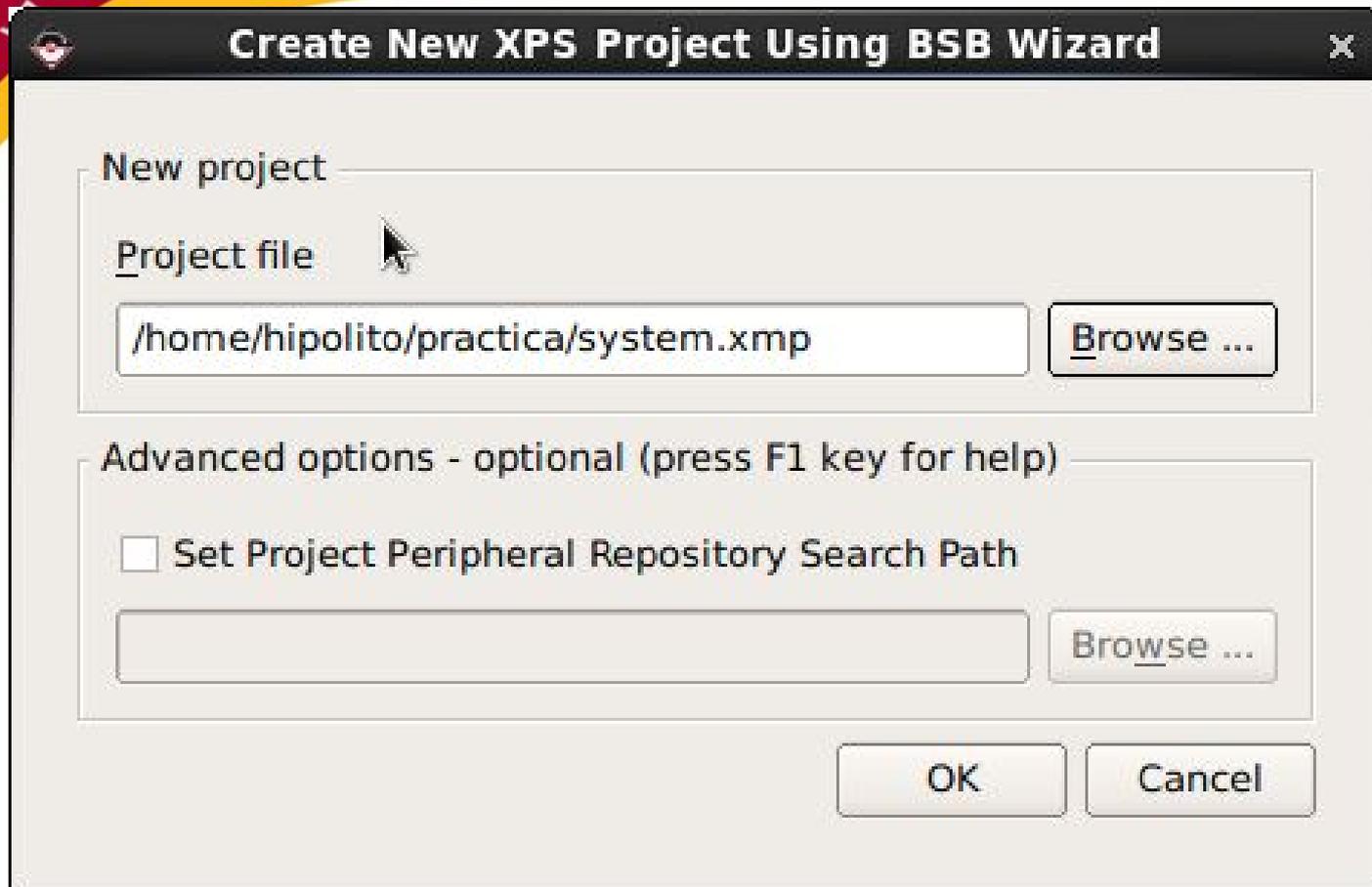


# Creación del proyecto EDK

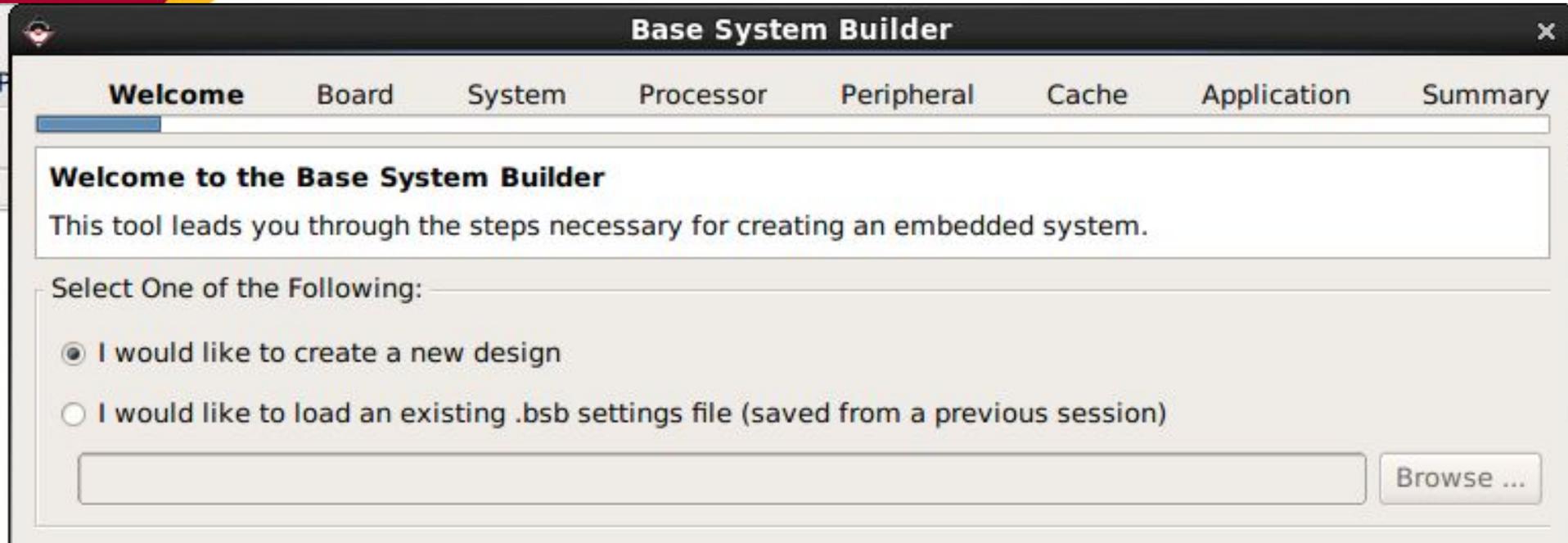


Elegimos Base System Builder Wizard

# Creación del proyecto EDK



Seleccionamos dónde se guardará el proyecto



Seleccionamos “I would like to create a new design”

**Base System Builder**

Welcome **Board** System Processor Peripheral Cache Application Summary

### Board Selection

Select a target development board.

Board

I would like to create a system for the following development board

Board Vendor: Avnet

Board Name: Avnet Spartan-6 LX9 MicroBoard

Board Revision: B

I would like to create a system for a custom board

### Board Information

Architecture	Device	Package	Speed Grade
spartan6	xc6slx9	csg324	-2

Use Stepping

Reset Polarity: Active High

### Related Information

[Vendor's Website](#)

[Vendor's Contact Information](#)

[Third Party Board Definition Files Download Website](#)

The Avnet Spartan-6 LX9 MicroBoard utilizes a Xilinx Spartan-6 XC6SLX9-2CSG324 device. The board is a USB-stick form factor evaluation board that includes USB JTAG circuitry, Micron 512Mb LPDDR, Micron 128Mb multi-I/O SPI Flash, 4 leds, 4-bit DIP switch, a TI programmable clock chip, a 10/100 National Ethernet PHY, and a single-chip TI power management unit

[More Info](#)

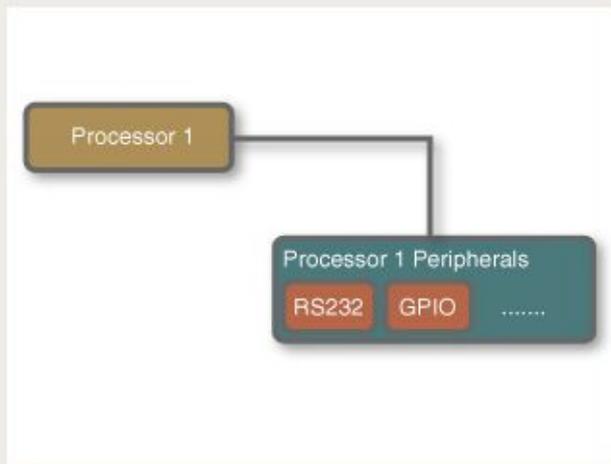
Seleccionar la tarjeta LX9 Microboard

**System Configuration**

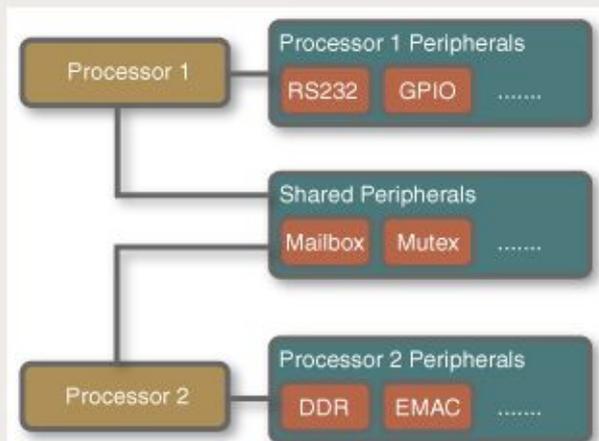
Configure your system.

 Single-Processor System

Select this option to create a design with a single processor. This Wizard will let you configure the processor, the peripheral set and some major configuration parameters for the peripherals.

 Dual-Processor System

Select this option to create a design with two processors. This Wizard will let you configure the types of the processors, the peripherals accessible to the two processors and the peripherals shared by the two processors.

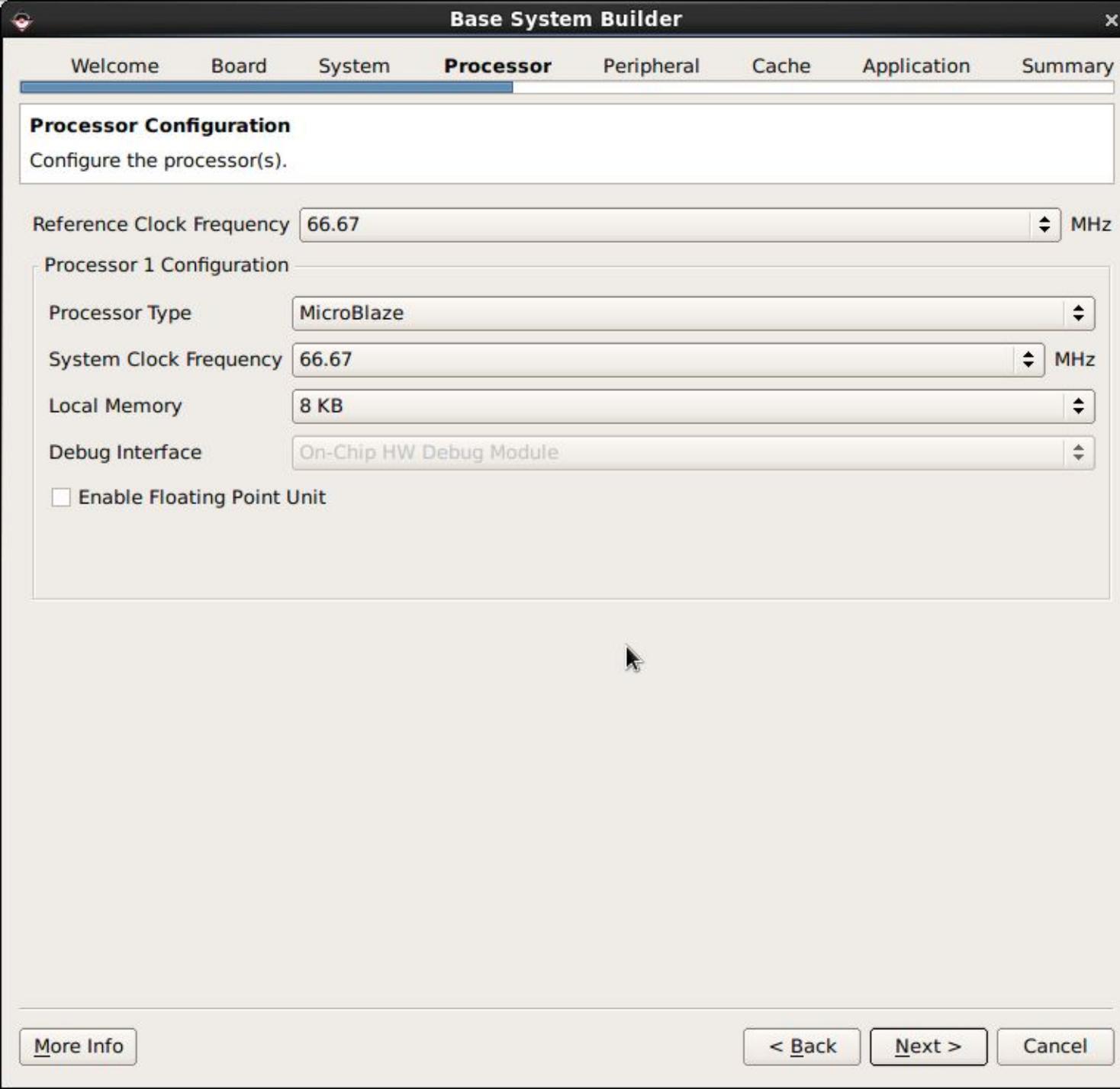
[More Info](#)

&lt; Back

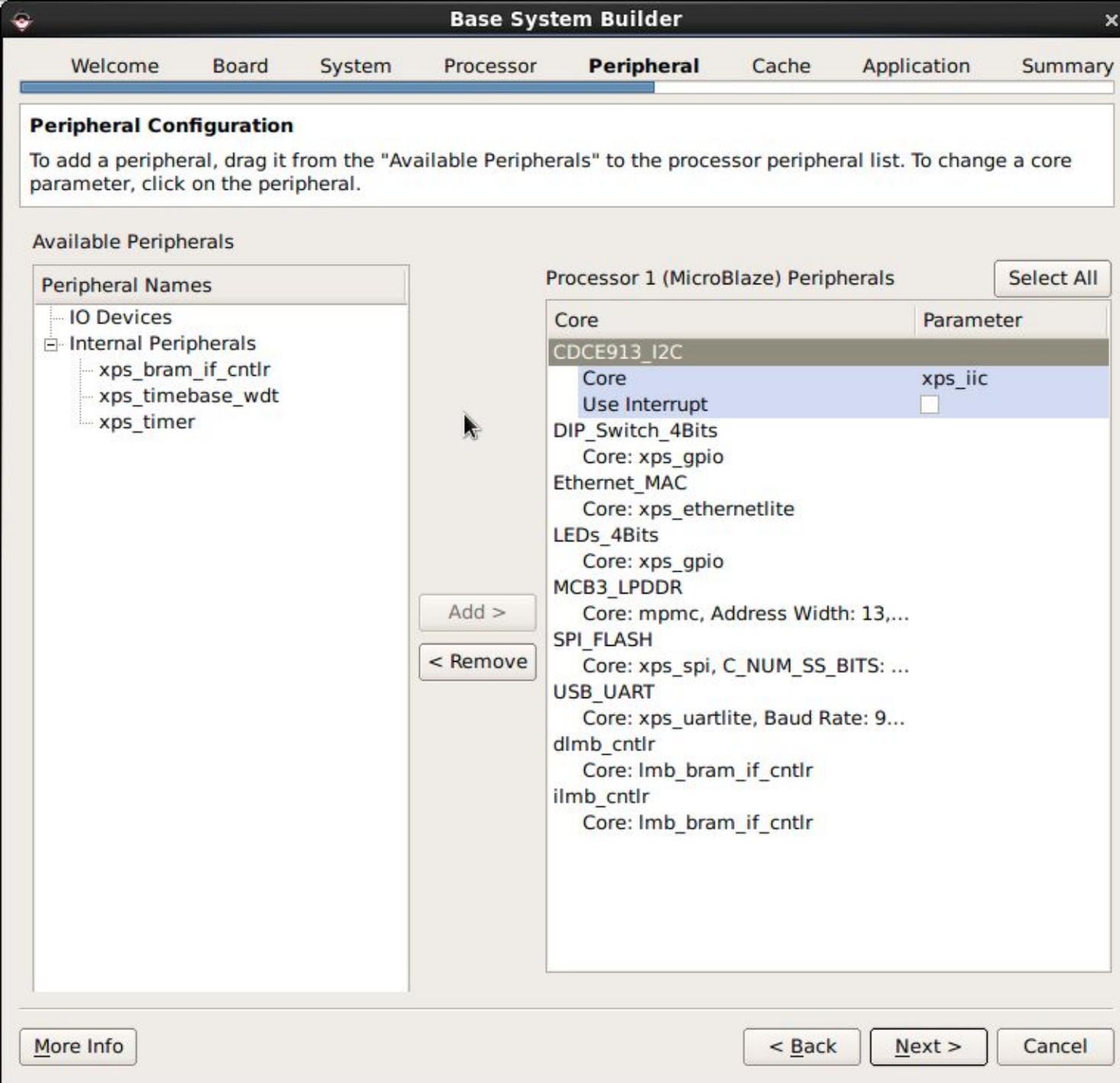
Next &gt;

Cancel

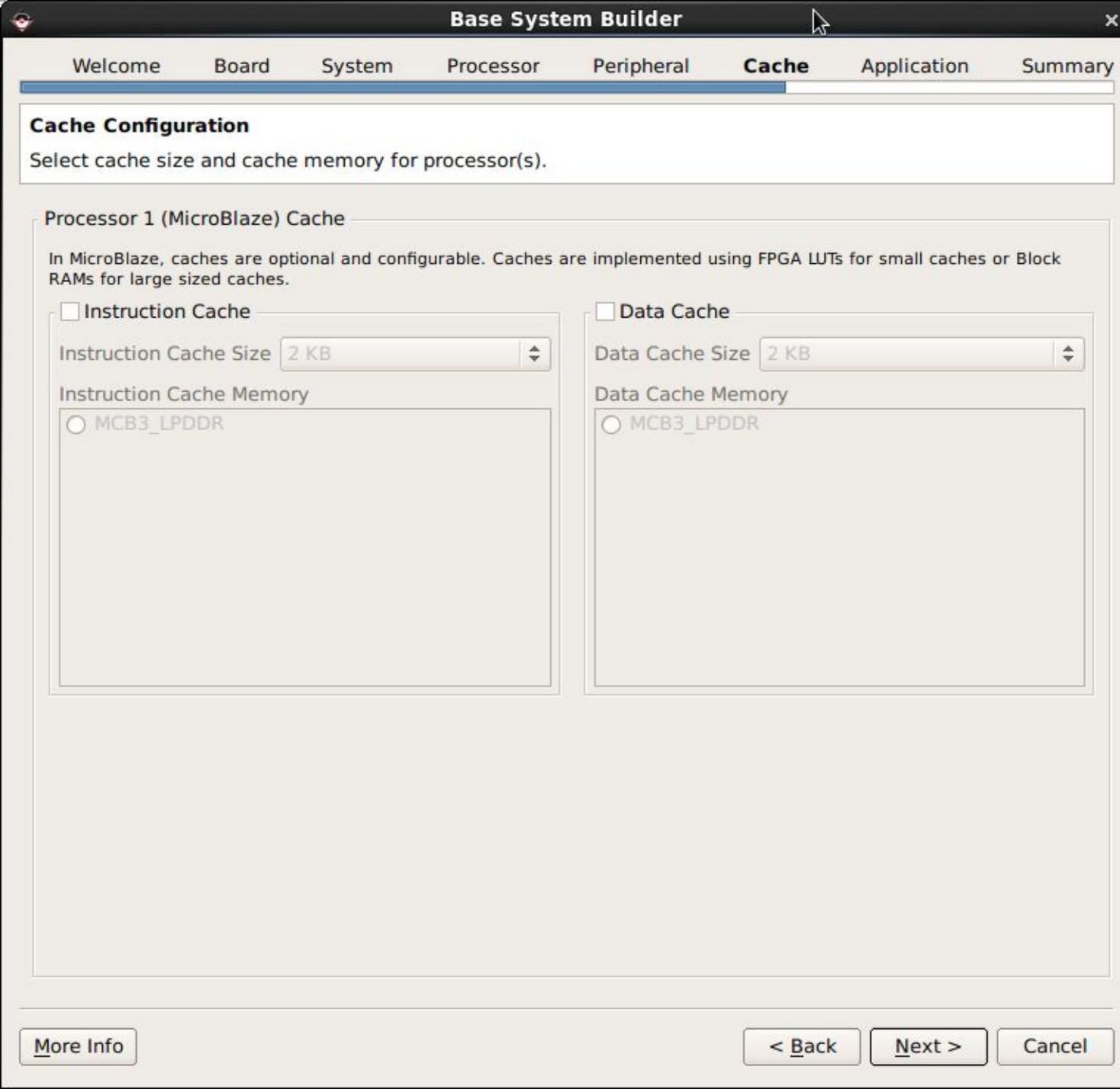
Seleccionar  
"Single  
Processor  
System"



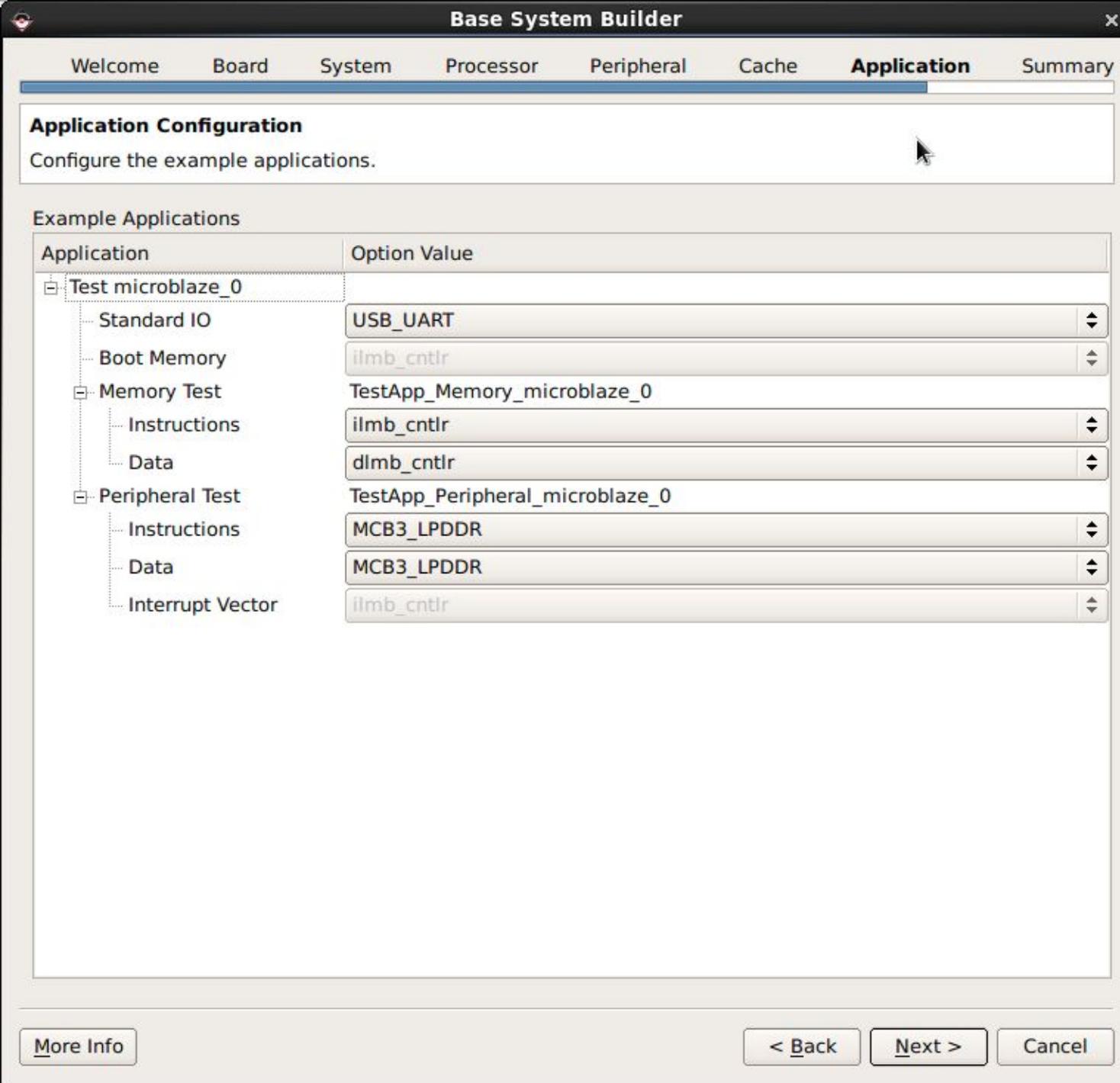
# Configuración del procesador



# Configuración de los periféricos



# Configuración de las memorias caché



## Application Configuration

Configure the example applications.

### Example Applications

Application	Option Value
[-] Test microblaze_0	
Standard IO	USB_UART
Boot Memory	ilmb_cntlr
[-] Memory Test	TestApp_Memory_microblaze_0
Instructions	ilmb_cntlr
Data	dlmb_cntlr
[-] Peripheral Test	TestApp_Peripheral_microblaze_0
Instructions	MCB3_LPDDR
Data	MCB3_LPDDR
Interrupt Vector	ilmb_cntlr

Configuración de las aplicaciones

Nótese:  
stdio = UART  
Instruction y data memory = BRAMs o DDR externa

[More Info](#)

< Back

Next >

Cancel

**Summary**

Below is the summary of the system you are creating.

## System Summary

Core Name	Instance Name	Base Address	High Address
Processor 1	microblaze_0		
xps_iic	CDCE913_I2C	0x81600000	0x8160FFFF
xps_gpio	DIP_Switch_4Bits	0x81420000	0x8142FFFF
xps_ethernetlite	Ethernet_MAC	0x81000000	0x8100FFFF
xps_gpio	LEDs_4Bits	0x81400000	0x8140FFFF
mpmc	MCB3_LPDDR	0x8C000000	0x8FFFFFFF
xps_spi	SPI_FLASH	0x83400000	0x8340FFFF
xps_uartlite	USB_UART	0x84000000	0x8400FFFF
lmb_bram_if_cntlr	dlmb_cntlr	0x00000000	0x00001FFF
lmb_bram_if_cntlr	ilmb_cntlr	0x00000000	0x00001FFF

Mapa de memoria

Resumen

## File Location

- Overall
  - /home/hipolito/practica/system.xmp
  - /home/hipolito/practica/system.mhs
  - /home/hipolito/practica/system.mss
  - /home/hipolito/practica/data/system.ucf
  - /home/hipolito/practica/etc/fast\_runtime.opt
  - /home/hipolito/practica/etc/download.cmd
  - /home/hipolito/practica/etc/bitgen.ut
- TestApp\_Memory\_microblaze\_0
- TestApp\_Peripheral\_microblaze\_0

Ficheros fuente  
(al repo del tirón ;)

Save Base System Builder (.bsb) Settings File

/home/hipolito/practica/system.bsb

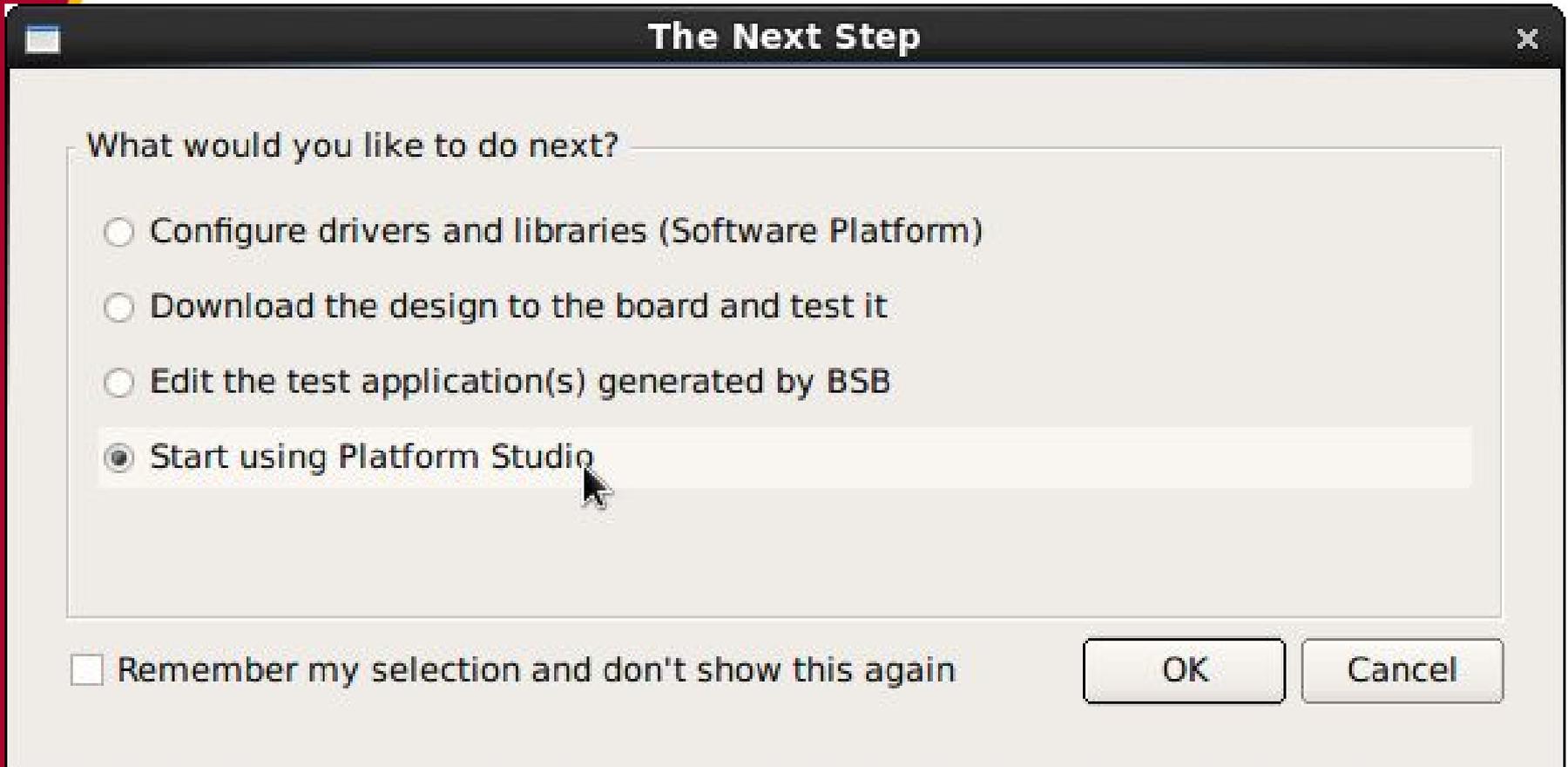
More Info

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Finish

Cancel

Seleccionamos 'Start using Platform Studio'



## Contenido

- Adición del BSP de la LX9 a EDK
- Creación del proyecto de EDK
- **Secciones importantes de EDK**
- Creación de un periférico GPIO

# Ventana principal de XPS

Xilinx Platform Studio - /home/hipolito/practica/system.xmp - [System Assembly View]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

Applications

Software Projects

- Add Software Application Project...
- Default: microblaze\_0\_bootloop
- Default: microblaze\_0\_xmdstub
- Project: TestApp\_Memory\_microblaze\_0**
  - Processor: microblaze\_0
  - Executable: /home/hipolito/practica/Te...
  - Compiler Options
  - Sources
  - Headers
- Project: TestApp\_Peripheral\_microblaze\_0**
  - Processor: microblaze\_0
  - Executable: /home/hipolito/practica/Te...
  - Compiler Options
  - Sources
  - Headers

Legend

- Master Slave Master/Slave Target Initiator Connected Unconnected
- Production License (paid) License (eval) Local Pre Production Beta Development
- Superseded Discontinued

Project Applications IP Catalog Design Summary Block Diagram System Assembly View

Console

```

Copied /home/hipolito/opt/Xilinx/12.1/ISE_DS/EDK/data/xflow/bitgen_spartan6.ut to etc directory
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 192 - PARAMETER C_MEM_DM_WIDTH ha
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 193 - PARAMETER C_MEM_DQS_WIDTH h
Generating Block Diagram to Buffer
/home/hipolito/opt/Xilinx/12.1/ISE_DS/EDK/data/xml/xslscripts/ConvertEdwardVersion.xsl
Generated Block Diagram SVG
    
```

Bus Interfaces Ports Addresses

Name	Bus Name	IP Type	IP Version
dmb		lmb_v10	1.00.a
ilmb		lmb_v10	1.00.a
mb_plb		plb_v46	1.04.a
microbla...		microblaze	7.30.a
lmb_bram		bram_bl...	1.00.a
dmb_cntlr		lmb_bra...	2.10.b
ilmb_cntlr		lmb_bra...	2.10.b
MCB3_LP...		mpmc	6.00.a
mdm_0		mdm	1.00.g
Ethernet...		xps_eth...	4.00.a
DIP_Swit...		xps_gpio	2.00.a
LEDs_4Bits		xps_gpio	2.00.a
CDCE913...		xps_iic	2.03.a
SPI_FLASH		xps_spi	2.01.b
USB_UART		xps_uart...	1.01.a

Bus Interface Filters

- By Connection
  - Connected
  - Unconnected
- By Bus Standard
  - LMB
  - PLBV46
  - FSL
  - Xilinx Point T...
- By Interface Type
  - Slaves
  - Masters
  - Master Slaves
  - Monitors
  - Targets
  - Initiators

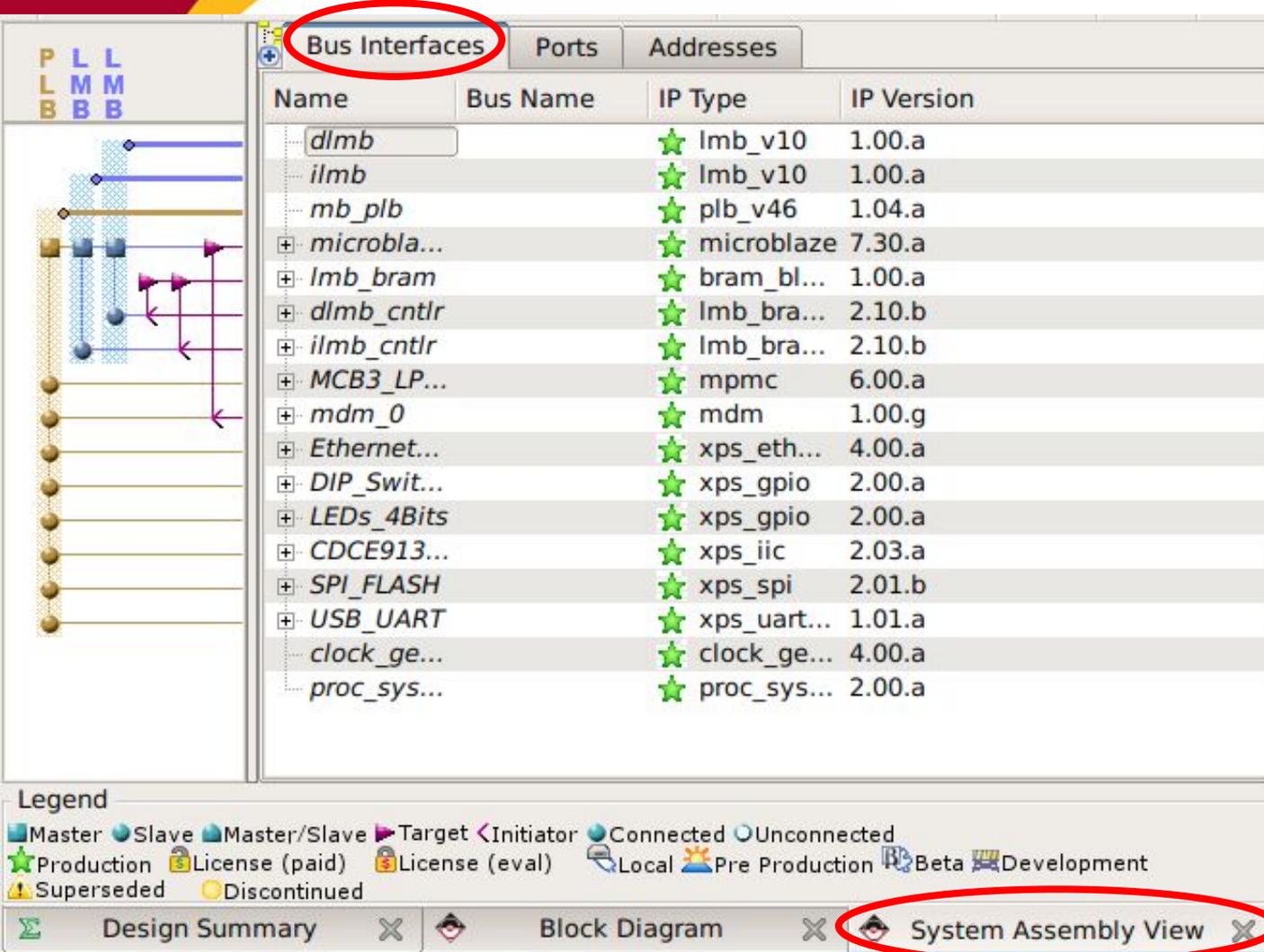
```
Console
Copied /home/hipolito/opt/Xilinx/12.1/ISE_DS/EDK/data/xflow/bitgen_spartan6.ut to etc directory
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 192 - PARAMETER C_MEM_DM_WIDTH ha
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 193 - PARAMETER C_MEM_DQS_WIDTH I
Generating Block Diagram to Buffer
/home/hipolito/opt/Xilinx/12.1/ISE_DS/EDK/data/xml/xslscripts/ConvertEdwardVersion.xsl
Generated Block Diagram SVG
```

Console Warnings Errors

Por la consola veremos los warnings y errores

## System Assembly View - Bus

## Interfaces



Name	Bus Name	IP Type	IP Version
dmb		★ lmb_v10	1.00.a
ilmb		★ lmb_v10	1.00.a
mb_plb		★ plb_v46	1.04.a
+ microbla...		★ microblaze	7.30.a
+ lmb_bram		★ bram_bl...	1.00.a
+ dmb_cntlr		★ lmb_bra...	2.10.b
+ ilmb_cntlr		★ lmb_bra...	2.10.b
+ MCB3_LP...		★ mpmc	6.00.a
+ mdm_0		★ mdm	1.00.g
+ Ethernet...		★ xps_eth...	4.00.a
+ DIP_Swit...		★ xps_gpio	2.00.a
+ LEDs_4Bits		★ xps_gpio	2.00.a
+ CDCE913...		★ xps_iic	2.03.a
+ SPI_FLASH		★ xps_spi	2.01.b
+ USB_UART		★ xps_uart...	1.01.a
clock_ge...		★ clock_ge...	4.00.a
proc_sys...		★ proc_sys...	2.00.a

Legend

- Master (blue square)
- Slave (blue circle)
- Master/Slave (blue diamond)
- Target (purple triangle)
- Initiator (pink triangle)
- Connected (blue circle)
- Unconnected (light blue circle)
- Production (green star)
- License (paid) (yellow lock)
- License (eval) (grey lock)
- Local (blue folder)
- Pre Production (orange star)
- Beta (blue star)
- Development (blue folder)
- Superseded (yellow triangle)
- Discontinued (yellow circle)

Design Summary | Block Diagram | System Assembly View

## System Assembly View - Ports

Bus Interfaces **Ports** Addresses + Add External Port

Name	Net	Direction	Range
<b>External Ports</b>			
fpga_0_USB_UART_RX_pin	fpga_0 U...	I	
fpga_0_USB_UART_TX_pin	fpga_0 U...	O	
fpga_0_LEDs_4Bits_GPIO_IO_O_pin	fpga_0 L...	O	[0:3]
fpga_0_DIP_Switch_4Bits_GPIO_IO_I_pin	fpga_0 D...	I	[0:3]
fpga_0_SPI_FLASH_SCK_pin	fpga_0 S...	I0	
fpga_0_SPI_FLASH_MISO_pin	fpga_0 S...	I0	
fpga_0_SPI_FLASH_MOSI_pin	fpga_0 S...	I0	
fpga_0_SPI_FLASH_SS_pin	fpga_0 S...	I0	
fpga_0_SPI_FLASH_SPI_HOLDn_pin	net_vcc	O	
fpga_0_SPI_FLASH_SPI_Wn_pin	net_vcc	O	
fpga_0_MCB3_LPDDR_mcbx_dram_addr_pin	fpga_0 M...	O	[12:0]
fpga_0_MCB3_LPDDR_mcbx_dram_ba_pin	fpga_0 M...	O	[1:0]
fpga_0_MCB3_LPDDR_mcbx_dram_ras_n_pin	fpga_0 M...	O	
fpga_0_MCB3_LPDDR_mcbx_dram_cas_n_pin	fpga_0 M...	O	
fpga_0_MCB3_LPDDR_mcbx_dram_we_n_pin	fpga_0 M...	O	
fpga_0_MCB3_LPDDR_mcbx_dram_cke_pin	fpga_0 M...	O	
fpga_0_MCB3_LPDDR_mcbx_dram_clk_pin	fpga_0 M...	O	

Legend

Master Slave Master/Slave Target Initiator Connected Unconnected  
Production License (paid) License (eval) Local Pre Production Beta Development  
Superseded Discontinued

Design Summary Block Diagram **System Assembly View**

## System Assembly View - Addresses (mapa de memoria)

Bus Interfaces | Ports | **Addresses** | Generate Addresses

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
microblaze_0's Address ...							
dlmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB	dlmb	<input type="checkbox"/>
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB	ilmb	<input type="checkbox"/>
Ethernet_MAC	C_BASEADDR	0x81000000	0x8100FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
LEDs_4Bits	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
DIP_Switch_4Bits	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
CDCE913_I2C	C_BASEADDR	0x81600000	0x8160FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
SPI_FLASH	C_BASEADDR	0x83400000	0x8340FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
USB_UART	C_BASEADDR	0x84000000	0x8400FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
MCB3_LPDDR	C_MPMC_BA...	0x8C000000	0x8FFFFFFF	64M	:SPLB0		<input type="checkbox"/>

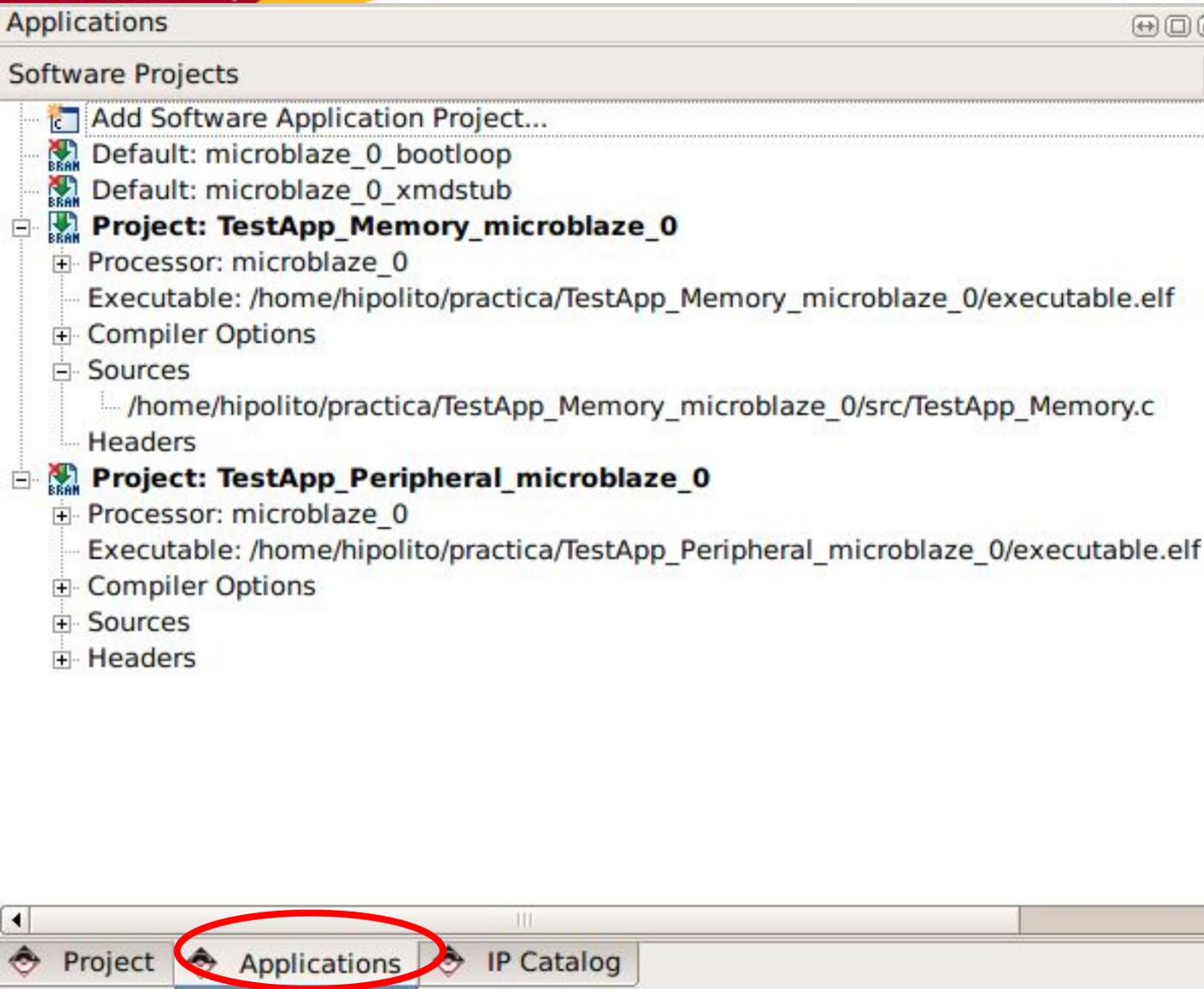
Legend

Master Slave Master/Slave Target Initiator Connected Unconnected  
Production License (paid) License (eval) Local Pre Production Beta Development  
Superseded Discontinued

Design Summary | Block Diagram | **System Assembly View**

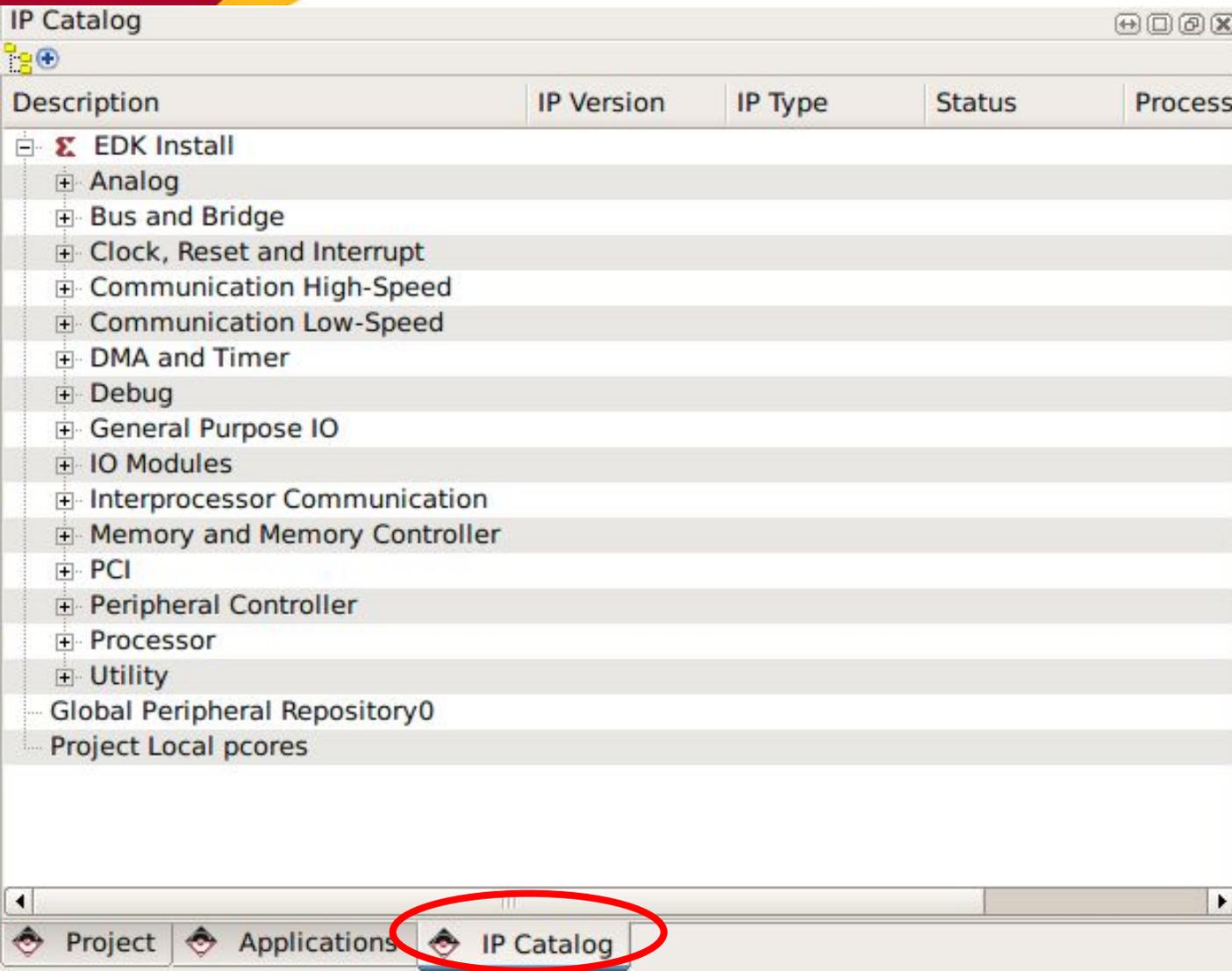


Project: Ficheros de configuración y opciones del proyecto



Applications:  
Aplicaciones  
software,  
códigos  
fuente y  
opciones de  
compilación

IP Catalog:  
Catálogo de  
IP cores  
(periféricos)  
para  
Microblaze



## Contenido

- Adición del BSP de la LX9 a EDK
- Creación del proyecto de EDK
- Secciones importantes de EDK
- **Creación de un periférico GPIO**

**system Project Status**

Project File:	system.xmp	Implementation State:	New
Module	system	Errors:	

**Añadimos un GPIO desde el IP Catalog**

**IP Catalog**

- EDK Install
- Analog
- Bus and Bridge
- Clock, Reset and Interrupt
- Communication High-Speed
- Communication Low-Speed
- DMA and Timer
- Debug
- General Purpose IO
- XPS General Purpose IO
- IO Modules
- Interprocessor Communication
- Memory and Memory Controller
- PCI
- Peripheral Controller
- Processor
- Utility
- Global Peripheral Repository0
- Project Local pcores

**Design Overview**

- Summary
- IOB Properties
- Module Level Utilization
- Timing Constraints
- Pinout Report
- Clock Report
- XPS Errors and Warnings
- Platgen Messages
- Libgen Messages
- Simgen Messages
- Bitlnit Messages
- XPS Reports

**Context Menu:**

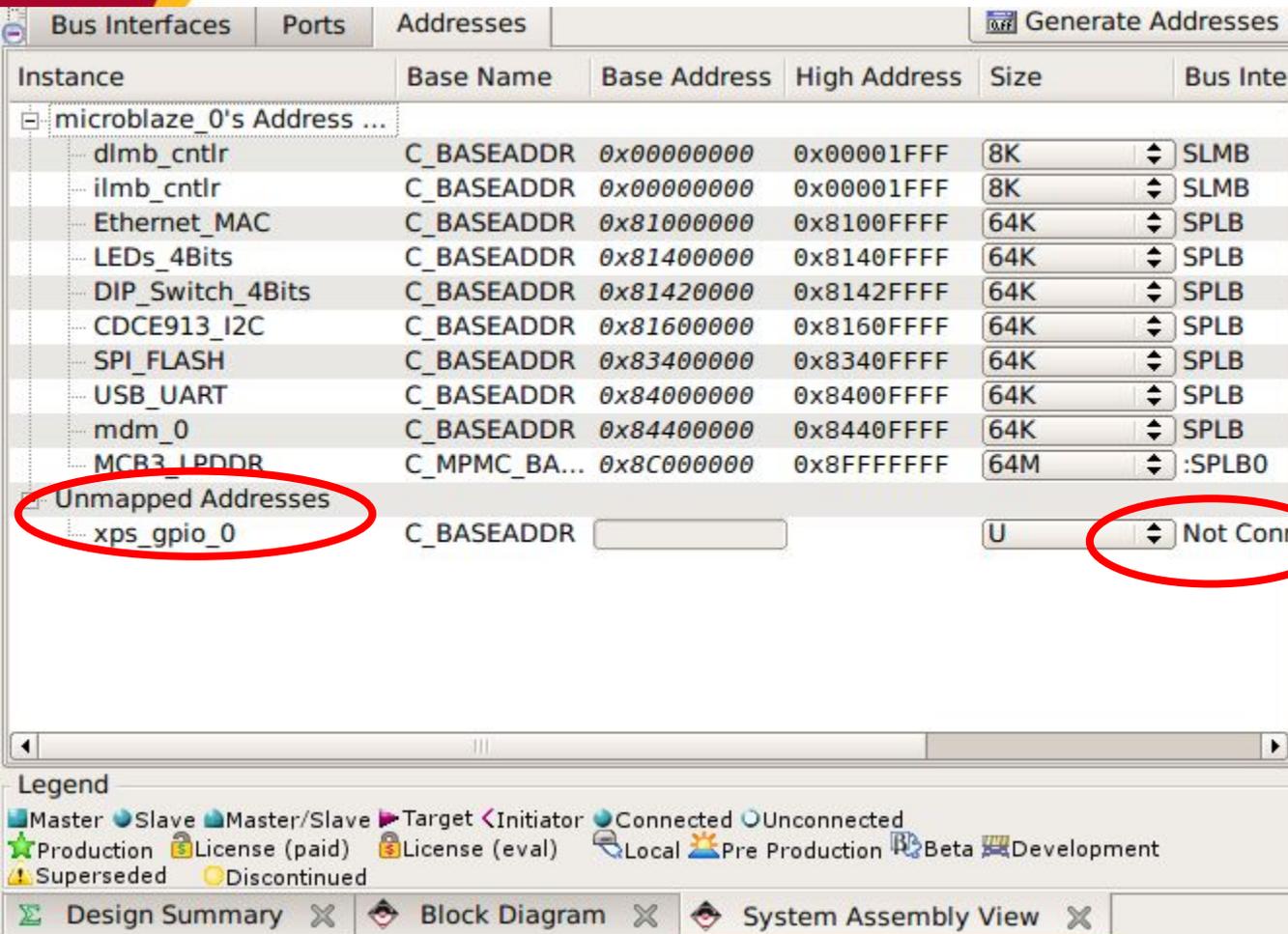
- Add IP
- View MPD
- View IP Modifications (Change Log)
- View PDF Datasheet
- Make This IP Local

**Console**

```
Copied /home/hipolito/opt/Xilinx/12.1/ISE_DS/EDK/data/xflow/bitgen/spartan6.ut to etc directory
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 192 - PARAMETER C_MEM_DM_WIDTH ha
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 193 - PARAMETER C_MEM_DQS_WIDTH I
Generating Block Diagram to Buffer
/home/hipolito/opt/Xilinx/12.1/ISE_DS/EDK/data/xml/xslscripts/ConvertEdwardVersion.xsl
```

# Creación de un periférico GPIO

Que esté en 'Unmapped Addresses' significa que no está accesible en el mapa de memoria



Instance	Base Name	Base Address	High Address	Size	Bus Inte
microblaze_0's Address ...					
dlmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB
Ethernet_MAC	C_BASEADDR	0x81000000	0x8100FFFF	64K	SPLB
LEDs_4Bits	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB
DIP_Switch_4Bits	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB
CDCE913_I2C	C_BASEADDR	0x81600000	0x8160FFFF	64K	SPLB
SPI_FLASH	C_BASEADDR	0x83400000	0x8340FFFF	64K	SPLB
USB_UART	C_BASEADDR	0x84000000	0x8400FFFF	64K	SPLB
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64K	SPLB
MCR3_LPDDR	C_MPMC_BA...	0x8C000000	0x8FFFFFFF	64M	:SPLB0
Unmapped Addresses					
xps_gpio_0	C_BASEADDR			U	Not Conn

Legend

Master Slave Master/Slave Target Initiator Connected Unconnected  
Production License (paid) License (eval) Local Pre Production Beta Development  
Superseded Discontinued

Design Summary | Block Diagram | System Assembly View

Not connected to SPLB (or any other bus)

Renombramos el nuevo periférico...

Name	Bus Name	IP Type	IP Version
dlmb		★ lmb_v10	1.00.a
ilmb		★ lmb_v10	
mb_plb		★ plb_v46	
microblaze_0		★ microblaze	
lmb_bram		★ bram_bl...	
dlmb_cntlr		★ lmb_bra...	
ilmb_cntlr		★ lmb_bra...	
MCB3_LPDDR		★ mpmc	
mdm_0		★ mdm	
Ethernet_MAC		★ xps_eth...	
DIP_Switch_4Bits		★ xps_gpio	
LEDs_4Bits		★ xps_gpio	
gpio_keypad		★ xps_gpio	
SPLB	No Conne...		
CDCE913_12C		★ xps_iic	
SPI_FLASH		★ xps_spi	
USB_UART		★ xps_uart...	1.01.a
clock_generator_0		★ clock_ge...	4.00.a
proc_sys_reset_0		★ proc_sys...	2.00.a

Legend

- Master (blue square), Slave (green circle), Master/Slave (purple triangle), Target (pink diamond), Initiator (blue circle), Connected (blue circle), Unconnected (white circle)
- ★ Production, License (paid) (yellow circle), License (eval) (orange circle), Local (blue circle), Pre Production (orange circle), Beta (blue circle), Development (blue circle)
- ⚠ Superseded, ⚪ Discontinued

Console

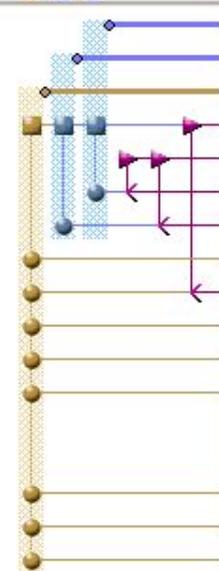
```
Generated Block Diagram SVG
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 192 - PARAMETER C_MEM_DM_WIDTH ha
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 193 - PARAMETER C_MEM_DQS_WIDTH I
WARNING:EDK:2137 - Peripheral gpio_keypad is not accessible from any processor in the system. Check Bus Interface connections ar
```



IP Catalog

Description

- EDK Install
- Analog
- Bus and Bridge
- Clock, Reset and Power
- Communications
- Communications
- DMA and Timers
- Debug
- General Purpose
- XPS General Purpose
- IO Modules
- Interprocessor
- Memory and Memory
- PCI
- Peripheral Controller
- Processor
- Utility
- Global Peripheral
- Project Local peripheral

P L L  
L M M  
B B B

Bus Interfaces Ports Addresses

Name	Bus Name	IP Type	IP Version
dlmb		★ lmb_v10	1.00.a
ilmb		★ lmb_v10	
mb_plb		★ plb_v46	
microblaze_0		★ microblaze	
lmb_bram		★ bram_bl...	
dlmb_cntlr		★ lmb_bra...	
ilmb_cntlr		★ lmb_bra...	
MCB3_LPDDR		★ mpmc	
mdm_0		★ mdm	
Ethernet_MAC		★ xps_eth...	
DIP_Switch_4Bits		★ xps_gpio	
LEDs_4Bits		★ xps_gpio	
gpio_keypad		★ xps_gpio	
SPLB			
CDCE913_I2C		★ iic	
SPI_FLASH		★ spi	
USB_UART		★ uart...	1.01.a
clock_generator_0		★ clock_ge...	4.00.a
proc_sys_reset_0		★ proc_sys...	2.00.a

Bus Interface Filters

- By Connection
- Connected

...Y lo conectamos al bus plb

Legend

- Master Slave Master/Slave Target Initiator Connected Unconnected
- ★ Production License (paid) License (eval) Local Pre Production Beta Development
- ⚠ Superseded Discontinued

IP Cat... Design Summary Block Diagram System Assembly View

Console

Generated Block Diagram SVG

- ⚠ WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3\_LPDDR - /home/hipolito/practica/system.mhs line 192 - PARAMETER C\_MEM\_DM\_WIDTH ha
- ⚠ WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3\_LPDDR - /home/hipolito/practica/system.mhs line 193 - PARAMETER C\_MEM\_DQS\_WIDTH I
- ⚠ WARNING:EDK:2137 - Peripheral gpio\_keypad is not accessible from any processor in the system. Check Bus Interface connections ar

Console Warnings Errors

Se puede apreciar que está conectado al bus

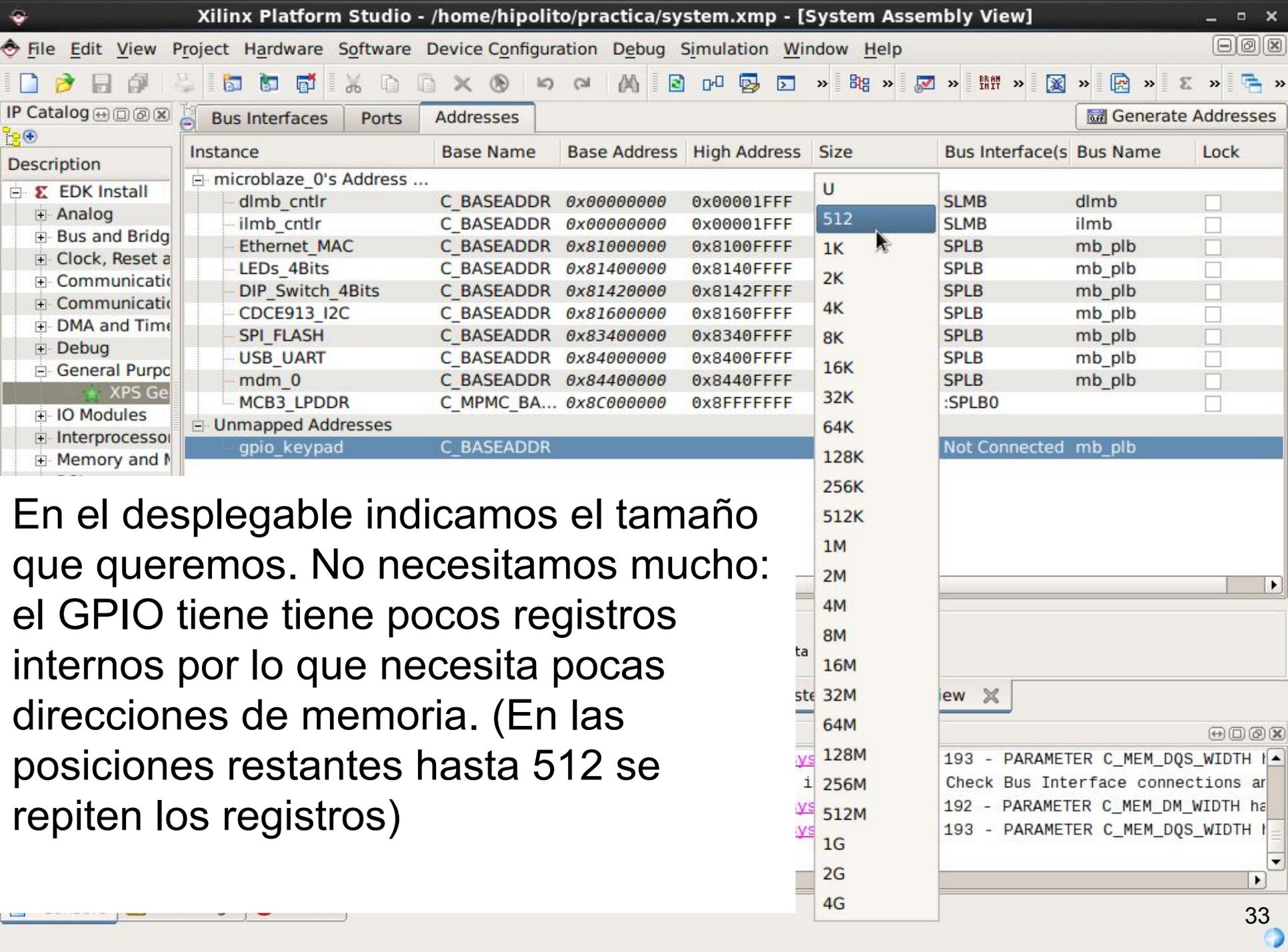
Name	Bus Name	IP Type	IP Version
dlmb		★ lmb_v10	1.00.a
ilmb		★ lmb_v10	1.00.a
mb_plb		★ plb_v46	1.00.a
microblaze_0		★ microblaze	1.00.a
lmb_bram		★ bram_bl...	1.00.a
dlmb_cntlr		★ lmb_bra...	2.00.a
ilmb_cntlr		★ lmb_bra...	2.00.a
MCB3_LPDDR		★ mpmc	6.00.a
mdm_0		★ mdm	1.00.a
Ethernet_MAC		★ xps_eth...	4.00.a
DIP_Switch_4Bits		★ xps_gpio	2.00.a
LEDs_4Bits		★ xps_gpio	2.00.a
gpio_keypad		★ xps_gpio	2.00.a
SPLB	mb_plb		
CDCE913_I2C		★ xps_iic	2.00.a
SPI_FLASH		★ xps_spi	2.00.a
USB_UART		★ xps_uart...	1.01.a
clock_generator_0		★ clock_ge...	4.00.a
proc_sys_reset_0		★ proc_sys...	2.00.a

Legend

- Master Slave Master/Slave Target Initiator Connected Unconnected
- ★ Production License (paid) License (eval) Local Pre Production Beta Development
- ⚠ Superseded ● Discontinued

Console

```
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 193 - PARAMETER C_MEM_DQS_WIDTH I
WARNING:EDK:2137 - Peripheral gpio_keypad is not accessible from any processor in the system. Check Bus Interface connections ar
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 192 - PARAMETER C_MEM_DM_WIDTH ha
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 193 - PARAMETER C_MEM_DQS_WIDTH I
```



IP Catalog

Description

- EDK Install
- Analog
- Bus and Bridge
- Clock, Reset and Power
- Communications
- Communications
- DMA and Timers
- Debug
- General Purpose
- XPS General Purpose
- IO Modules
- Interprocessor Communication
- Memory and Memory Controller

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
microblaze_0's Address ...							
dlmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	U	SLMB	dlmb	<input type="checkbox"/>
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	512	SLMB	ilmb	<input type="checkbox"/>
Ethernet_MAC	C_BASEADDR	0x81000000	0x8100FFFF	1K	SPLB	mb_plb	<input type="checkbox"/>
LEDs_4Bits	C_BASEADDR	0x81400000	0x8140FFFF	2K	SPLB	mb_plb	<input type="checkbox"/>
DIP_Switch_4Bits	C_BASEADDR	0x81420000	0x8142FFFF	2K	SPLB	mb_plb	<input type="checkbox"/>
CDCE913_I2C	C_BASEADDR	0x81600000	0x8160FFFF	4K	SPLB	mb_plb	<input type="checkbox"/>
SPI_FLASH	C_BASEADDR	0x83400000	0x8340FFFF	8K	SPLB	mb_plb	<input type="checkbox"/>
USB_UART	C_BASEADDR	0x84000000	0x8400FFFF	16K	SPLB	mb_plb	<input type="checkbox"/>
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	16K	SPLB	mb_plb	<input type="checkbox"/>
MCB3_LPDDR	C_MPMC_BA...	0x8C000000	0x8FFFFFFF	32K	:SPLB0		<input type="checkbox"/>

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
Unmapped Addresses							
gpio_keypad	C_BASEADDR			128K	Not Connected	mb_plb	

- U
- 512
- 1K
- 2K
- 4K
- 8K
- 16K
- 32K
- 64K
- 128K
- 256K
- 512K
- 1M
- 2M
- 4M
- 8M
- 16M
- 32M
- 64M
- 128M
- 256M
- 512M
- 1G
- 2G
- 4G

193 - PARAMETER C\_MEM\_DQS\_WIDTH I  
Check Bus Interface connections ar  
192 - PARAMETER C\_MEM\_DM\_WIDTH ha  
193 - PARAMETER C\_MEM\_DQS\_WIDTH I

En el desplegable indicamos el tamaño que queremos. No necesitamos mucho: el GPIO tiene pocos registros internos por lo que necesita pocas direcciones de memoria. (En las posiciones restantes hasta 512 se repiten los registros)

Xilinx Platform Studio - /home/hipolito/practica/system.xmp - [System Assembly View]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

IP Catalog Bus Interfaces Ports Addresses Generate Addresses

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
microblaze_0's Address ...							
dmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB	dmb	<input type="checkbox"/>
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB	ilmb	<input type="checkbox"/>
gpio_keypad	C_BASEADDR	0x00000000	0x000001FF	512	SPLB	mb_plb	<input checked="" type="checkbox"/>
Ethernet_MAC	C_BASEADDR	0x81000000	0x8100FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
LEDs_4Bits	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
DIP_Switch_4Bits	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
CDCE913_I2C	C_BASEADDR	0x81600000	0x8160FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
SPI_FLASH	C_BASEADDR	0x83400000	0x8340FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
USB_UART	C_BASEADDR	0x84000000	0x8400FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
MCB3_LPDDR	C_MPMC_BA...	0x8C000000	0x8FFFFFFF	64M	:SPLB0		<input type="checkbox"/>

EDK Install  
Analog  
Bus and Bridg  
Clock, Reset a  
Communicati  
Communicati  
DMA and Time  
Debug  
General Purpc  
XPS Ge  
IO Modules  
Interprocesso

Ahora aparece en el mapa de memoria de microblaze, pero nos da errores porque el baseaddr 0x0 solapa con las memorias de datos e instrucciones

IP Cat... Design Summary Block Diagram System Assembly View

Console

```

ERROR:EDK:1519 - INST:dmb_cntlr BASEADDR-HIGHADDR:0000000000-0x00001fff and INST:gpio_keypad BASEADDR-HIGHADDR:0000000000-0x
ERROR:EDK:1519 - INST:ilmb_cntlr BASEADDR-HIGHADDR:0000000000-0x00001fff and INST:gpio_keypad BASEADDR-HIGHADDR:0000000000-0x
ERROR:EDK:1519 - INST:gpio_keypad BASEADDR-HIGHADDR:0000000000-0x000001ff and INST:dmb_cntlr BASEADDR-HIGHADDR:0000000000-0x
ERROR:EDK:1519 - INST:gpio_keypad BASEADDR-HIGHADDR:0000000000-0x000001ff and INST:ilmb_cntlr BASEADDR-HIGHADDR:0000000000-0x

```

Console Warnings Errors

Xilinx Platform Studio - /home/hipolito/practica/system.xmp - [System Assembly View]

File Edit View Project Hardware Software Device Configuration Debug Simulation Window Help

IP Catalog Bus Interfaces Ports Addresses Generate Addresses

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name	Lock
microblaze_0's Address ...							
dlmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB	dlmb	<input type="checkbox"/>
ilmb_cntlr	C_BASEADDR	0x00000000	0x00001FFF	8K	SLMB	ilmb	<input type="checkbox"/>
Ethernet_MAC	C_BASEADDR	0x81000000	0x8100FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
LEDs_4Bits	C_BASEADDR	0x81400000	0x8140FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
DIP_Switch_4Bits	C_BASEADDR	0x81420000	0x8142FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
CDCE913_I2C	C_BASEADDR	0x81600000	0x8160FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
gpio_keypad	C_BASEADDR	0x81700000	0x817001FF	512	SPLB	mb_plb	<input type="checkbox"/>
SPI_FLASH	C_BASEADDR	0x83400000	0x8340FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
USB_UART	C_BASEADDR	0x84000000	0x8400FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64K	SPLB	mb_plb	<input type="checkbox"/>
MCB3_LPDDR	C_MPMC_BA...	0x8C000000	0x8FFFFFFF	64M	:SPLB0		<input type="checkbox"/>

EDK Install  
 Analog  
 Bus and Bridg  
 Clock, Reset a  
 Communicatio  
 Communicatio  
 DMA and Time  
 Debug  
 General Purpc  
 XPS Ge  
 IO Modules  
 Interprocesso

Asignamos una dirección base tal que el rango de direcciones (desde dirección base hasta dirección base + tamaño) no solape con ningún otro elemento ya existente en el mapa de memoria

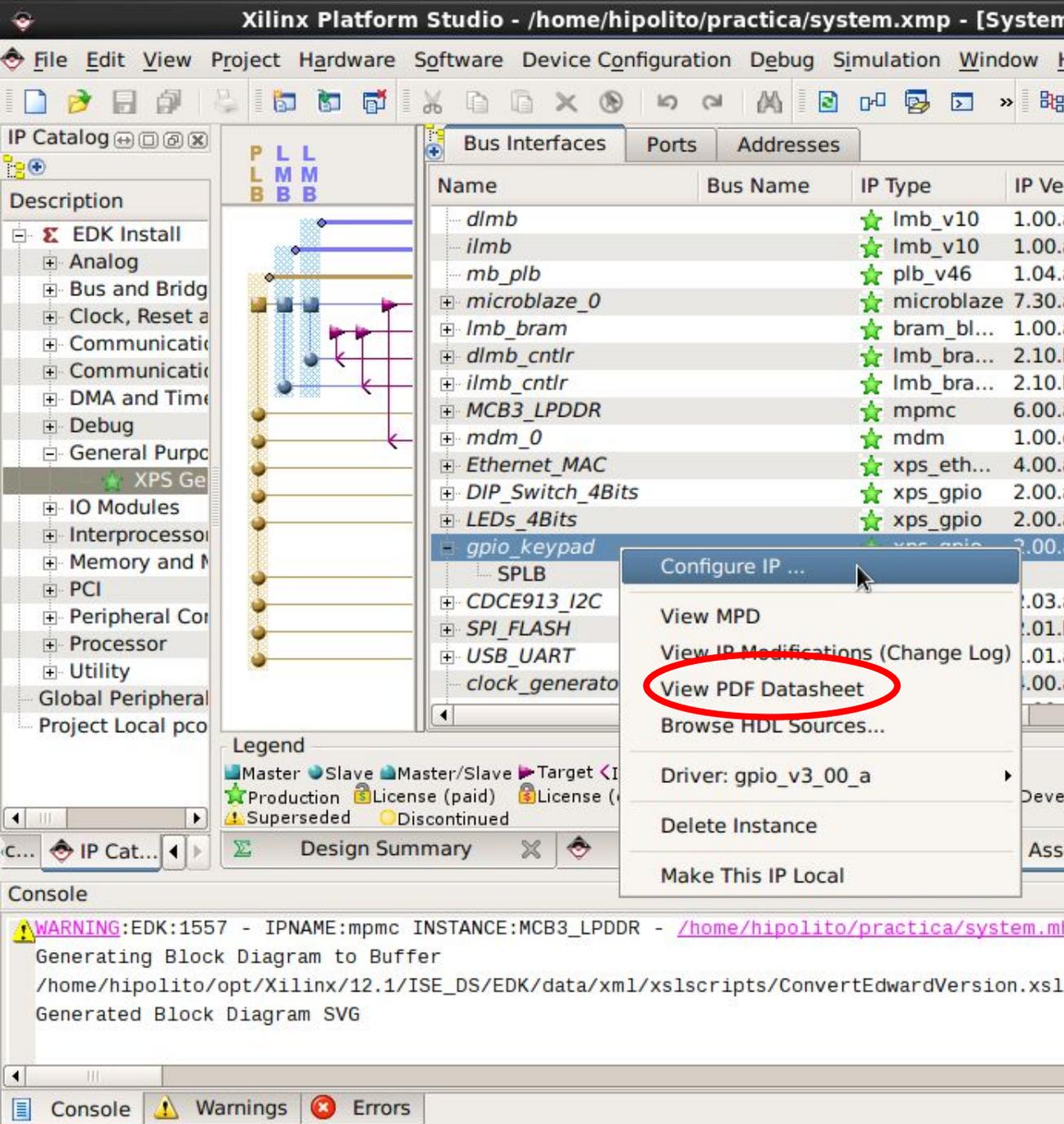
IP Cat... Design Summary Block Diagram System Assembly View

Console

```

ERROR:EDK:1519 - INST:gpio_keypad BASEADDR-HIGHADDR:0000000000-0x000001ff and INST:dlmb_cntlr BASEADDR-HIGHADDR:0000000000-0x000001ff
ERROR:EDK:1519 - INST:gpio_keypad BASEADDR-HIGHADDR:0000000000-0x000001ff and INST:ilmb_cntlr BASEADDR-HIGHADDR:0000000000-0x000001ff
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 192 - PARAMETER C_MEM_DM_WIDTH ha
WARNING:EDK:1557 - IPNAME:mpmc INSTANCE:MCB3_LPDDR - /home/hipolito/practica/system.mhs line 193 - PARAMETER C_MEM_DQS_WIDTH I
  
```

Console Warnings Errors



Ahora que tenemos el GPIO conectado al microblaze hacemos click derecho -> Configure IP ...

No os olvidéis de "View PDF Datasheet"

User System Buses

HDL



Common

Channel 1

Channel 2

GPIO Supports Interrupts Enable Channel 2 

Este menú es bastante auto-explicativo:

- Soporte para interrupciones
- Habilitar canal 2 del GPIO

OK

Cancel

Help

User System Buses

HDL PDF

Common  
Channel 1  
Channel 2

GPIO Data Channel Width 32

Channel 1 Data Out Default Value 0x00000000

Channel 1 Tri-state Default Value 0xffffffff

Channel 1 is Input Only FALSE

OK Cancel Help

## Configuramos:

- Anchura del GPIO
- Valor de salida / triestado por defecto
- Si el canal 1 es sólo entrada



- Este menú está 'grayed out' si no hemos habilitado el Canal 2
- La configuración más sencilla si necesitamos entradas y salidas es usar un canal sólo para las entradas y otro sólo para las salidas

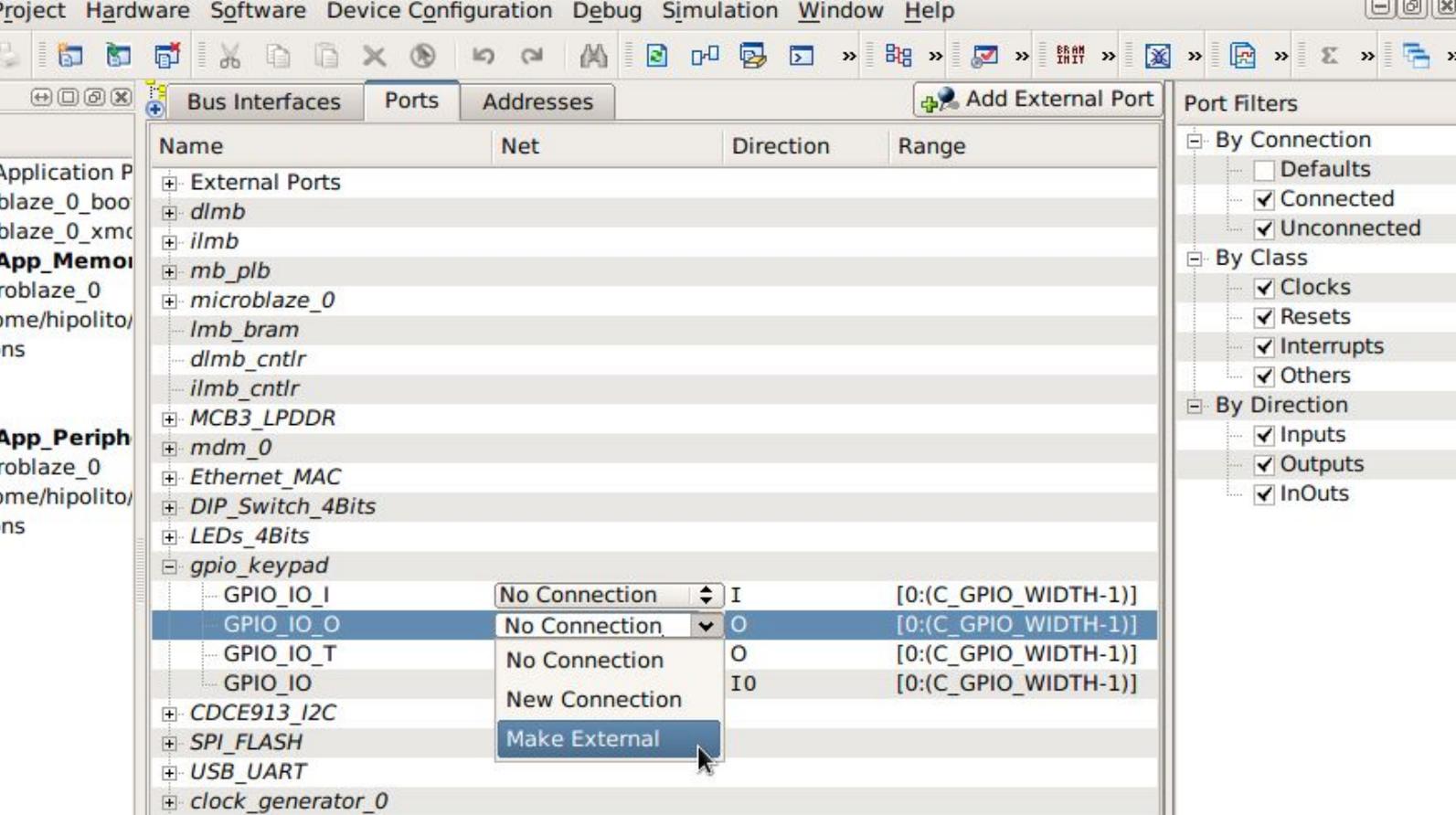
Name	Net	Direction	Range
------	-----	-----------	-------

External Ports			
dlmb			
ilmb			
mb_plb			
microblaze_0			
lmb_bram			
dlmb_cntlr			
ilmb_cntlr			
MCB3_LPDDR			
mdm_0			
Ethernet_MAC			
DIP_Switch_4Bits			
LEDs_4Bits			
gpio_keypad			
GPIO_IO_I	No Connection	I	[0:(C_GPIO_WIDTH-1)]
GPIO_IO_O	No Connection	O	[0:(C_GPIO_WIDTH-1)]
GPIO_IO_T	No Connection	O	[0:(C_GPIO_WIDTH-1)]
GPIO_IO	No Connection	I0	[0:(C_GPIO_WIDTH-1)]
CDCE913_I2C			
SPI_FLASH			
USB_UART			
clock_generator_0			
proc_sys_reset_0			

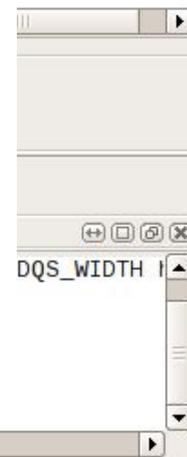
El periférico GPIO tiene por un lado el PLB y por el otro los pines de E/S de propósito general.

- `_IO_I` : Sólo Input
- `_IO_O` : Sólo Output
- `_IO` : Input/Output (bidireccional)
- `_IO_T` : Triestado (afecta a la bidireccional)

Por ahora estos pines están sin conectar a nada



En la entrada o salida del GPIO que vayamos a utilizar seleccionamos “Make External” para que se convierta en un puerto externo del procesador



Bus Interfaces

Ports

Addresses

Name

Net

+ External Ports

+ dlmb

+ ilmb

+ mb\_plb

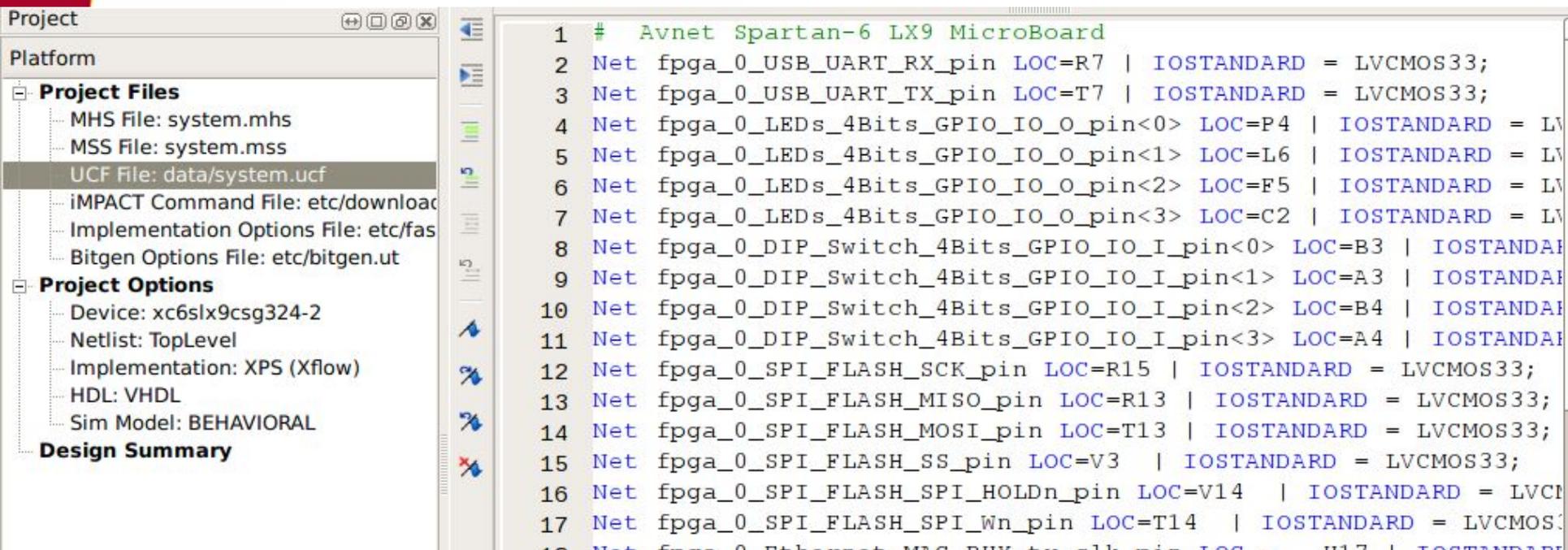
+ microblaze\_0

Abrimos External Ports, y veremos que hay un puerto nuevo del microprocesador, que corresponde a los pines del GPIO que hemos hecho externos

fpga_0_clk_1_sys_clk_pin	gen_clk_0	1	
fpga_0_rst_1_sys_rst_pin	sys_rst_s	I	
gpio_keypad_GPIO_IO_0_pin	gpio_keypad_GPIO_IO_0	0	[0:31]

Como ahora tenemos más pines en nuestro diseño, ¿no podemos olvidar añadirlos al UCF!

IOSTANDARD se refiere a los niveles de tensión de la E/S



The screenshot shows the Xilinx ISE software interface. On the left, the 'Project' window displays the 'Project Files' section, where the UCF file 'data/system.ucf' is highlighted. Below it, the 'Project Options' section shows the device 'xc6slx9csg324-2' and the implementation 'XPS (Xflow)'. The main window displays the UCF file content, which lists various pins and their IOSTANDARD settings.

```
1 # Avnet Spartan-6 LX9 MicroBoard
2 Net fpga_0_USB_UART_RX_pin LOC=R7 | IOSTANDARD = LVCMOS33;
3 Net fpga_0_USB_UART_TX_pin LOC=T7 | IOSTANDARD = LVCMOS33;
4 Net fpga_0_LEDs_4Bits_GPIO_IO_0_pin<0> LOC=P4 | IOSTANDARD = LVCMOS33;
5 Net fpga_0_LEDs_4Bits_GPIO_IO_0_pin<1> LOC=L6 | IOSTANDARD = LVCMOS33;
6 Net fpga_0_LEDs_4Bits_GPIO_IO_0_pin<2> LOC=F5 | IOSTANDARD = LVCMOS33;
7 Net fpga_0_LEDs_4Bits_GPIO_IO_0_pin<3> LOC=C2 | IOSTANDARD = LVCMOS33;
8 Net fpga_0_DIP_Switch_4Bits_GPIO_IO_I_pin<0> LOC=B3 | IOSTANDARD = LVCMOS33;
9 Net fpga_0_DIP_Switch_4Bits_GPIO_IO_I_pin<1> LOC=A3 | IOSTANDARD = LVCMOS33;
10 Net fpga_0_DIP_Switch_4Bits_GPIO_IO_I_pin<2> LOC=B4 | IOSTANDARD = LVCMOS33;
11 Net fpga_0_DIP_Switch_4Bits_GPIO_IO_I_pin<3> LOC=A4 | IOSTANDARD = LVCMOS33;
12 Net fpga_0_SPI_FLASH_SCK_pin LOC=R15 | IOSTANDARD = LVCMOS33;
13 Net fpga_0_SPI_FLASH_MISO_pin LOC=R13 | IOSTANDARD = LVCMOS33;
14 Net fpga_0_SPI_FLASH_MOSI_pin LOC=T13 | IOSTANDARD = LVCMOS33;
15 Net fpga_0_SPI_FLASH_SS_pin LOC=V3 | IOSTANDARD = LVCMOS33;
16 Net fpga_0_SPI_FLASH_SPI_HOLDn_pin LOC=V14 | IOSTANDARD = LVCMOS33;
17 Net fpga_0_SPI_FLASH_SPI_Wn_pin LOC=T14 | IOSTANDARD = LVCMOS33;
18 Net fpga_0_Ethernet_MAC_PU_V_tn_alk_pin LOC=U17 | IOSTANDARD = LVCMOS33;
```

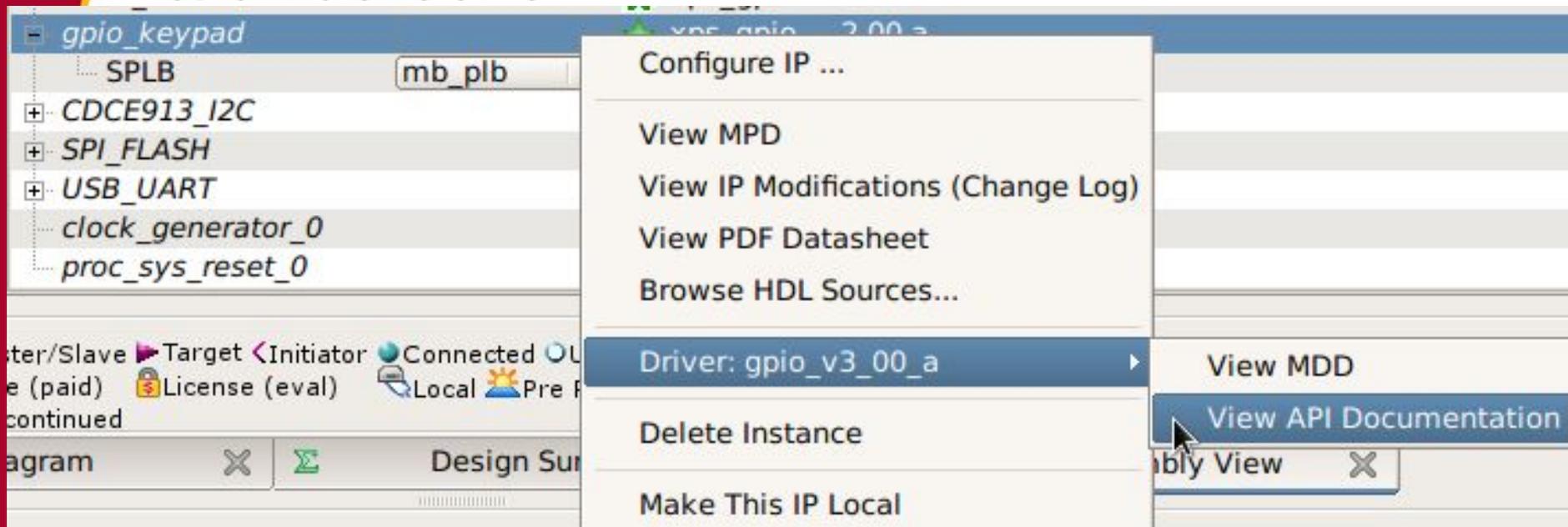
## Manejo por software

Ya tenemos el hardware, ahora necesitamos conocer las funciones para manejarlo

Estudiad cómo se manejan los leds escribiendo en el gpio *LEDs\_4bits* en el Proyecto *TestApp\_Peripheral\_microblaze\_0* (específicamente, en el fichero *xgpio\_tapp\_example.c*)

## Manejo por software

Podemos ver la API del Driver haciendo click derecho:



(si os fijáis, está hecha con un generador de documentación ;)