FPGA architecture

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Teaching context

B02: Advanced Programmable Logic Systems

- Tema 1: FPGA architecture
- Tema 2: Advanced digital design methodologies
- Tema 3: Advanced VHDL
- Tema 4: Verification capabilities for digital circuits

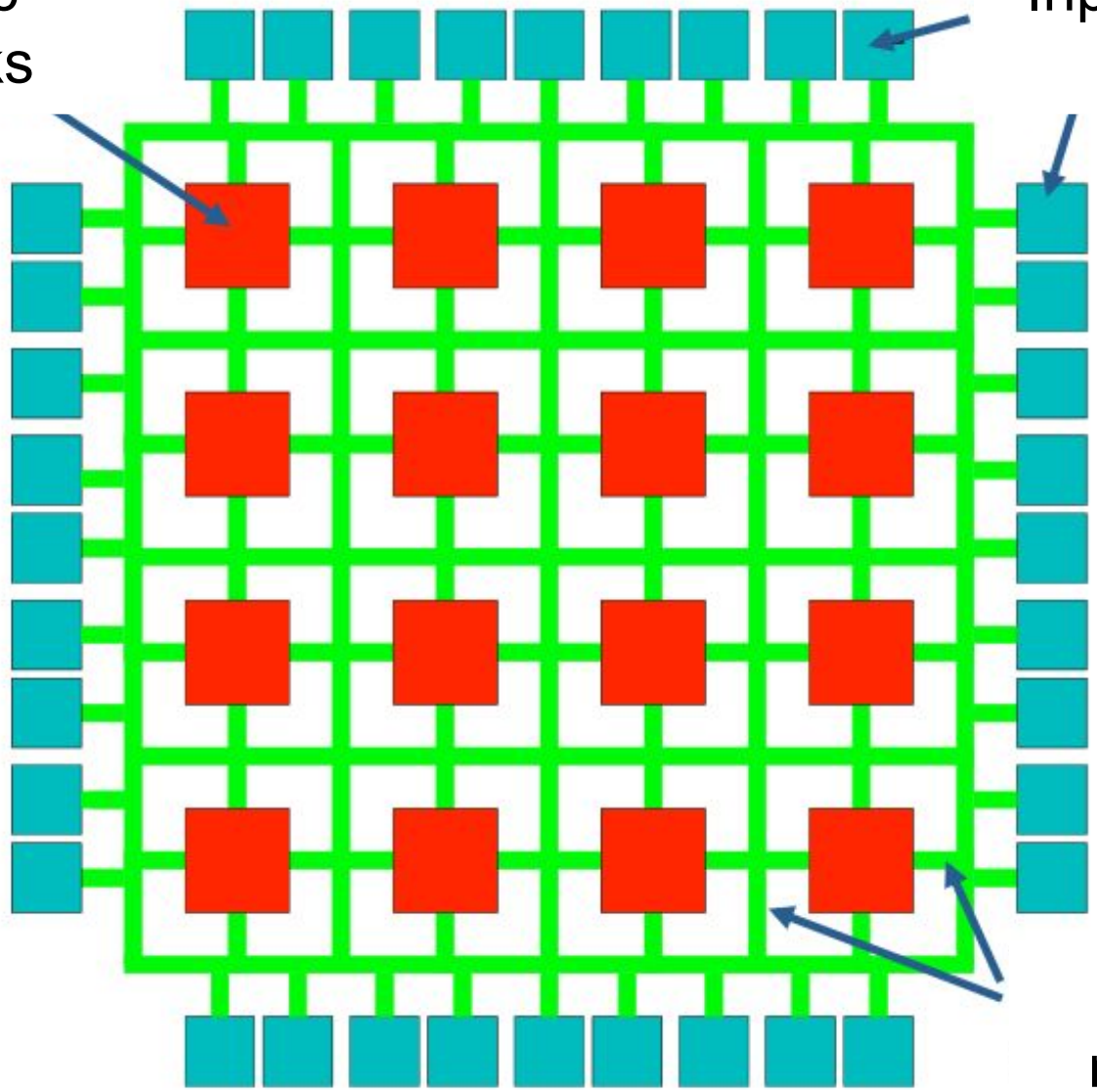
Required prior knowledge:

- Basic knowledge of digital design
  - Logic gates and flip-flops

Internal architecture of an FPGA

- IOBs: In/Out Blocks
- CLBs: Configurable Logic Blocks
- Routing Resources
- (Re)Programmability

FPGA architecture



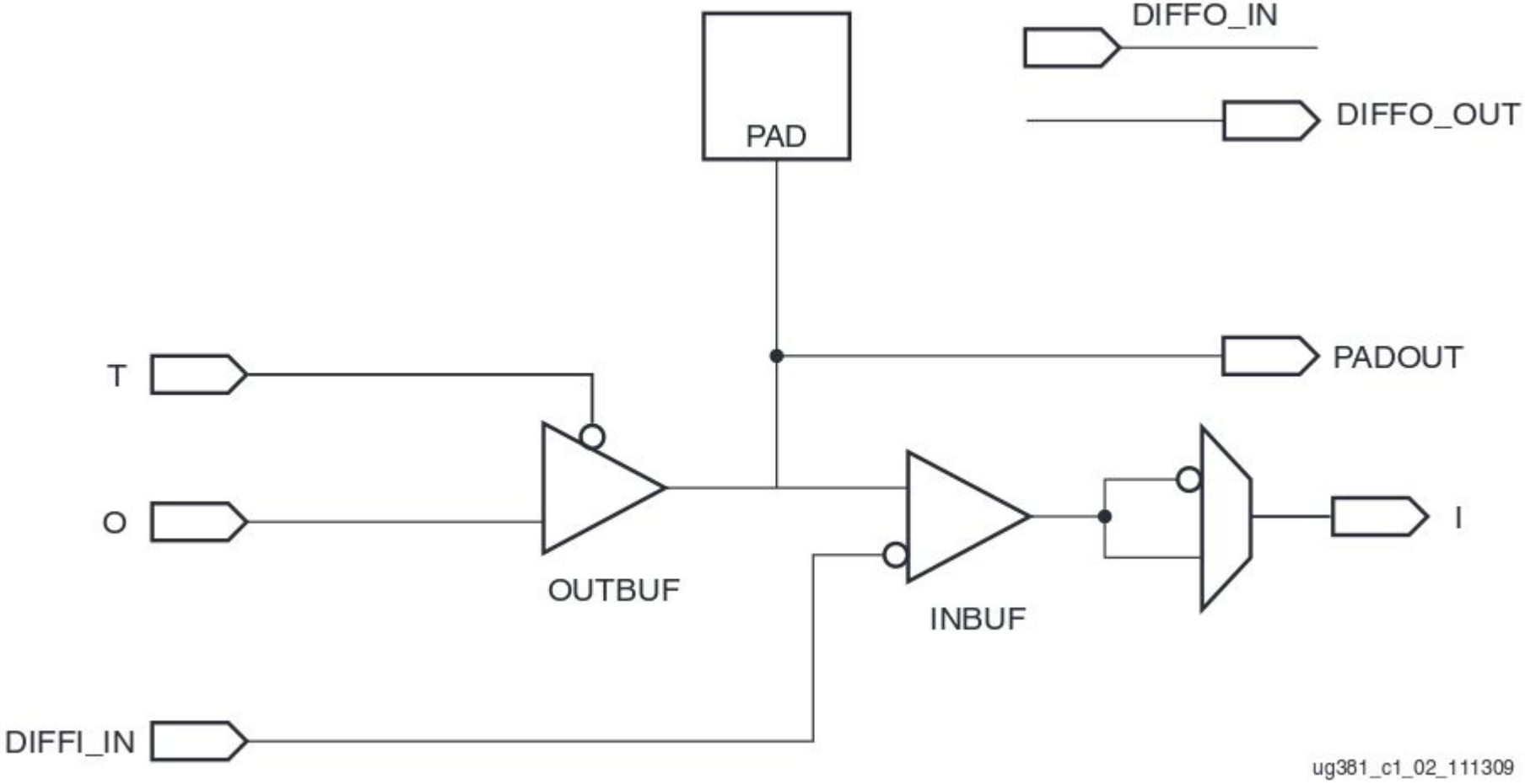
In-Out Blocks (IOBs)

- PAD (connection to the outside of the chip)
- Input buffer
- Output buffer (tri-state)

- Optionally: support for differential input/outputs (this depends on the FPGA family)

These are called IOBs in Xilinx technologies, other vendors just call them I/Os

IOB Spartan-6



Configurable Logic Blocks (CLBs)

Made of:

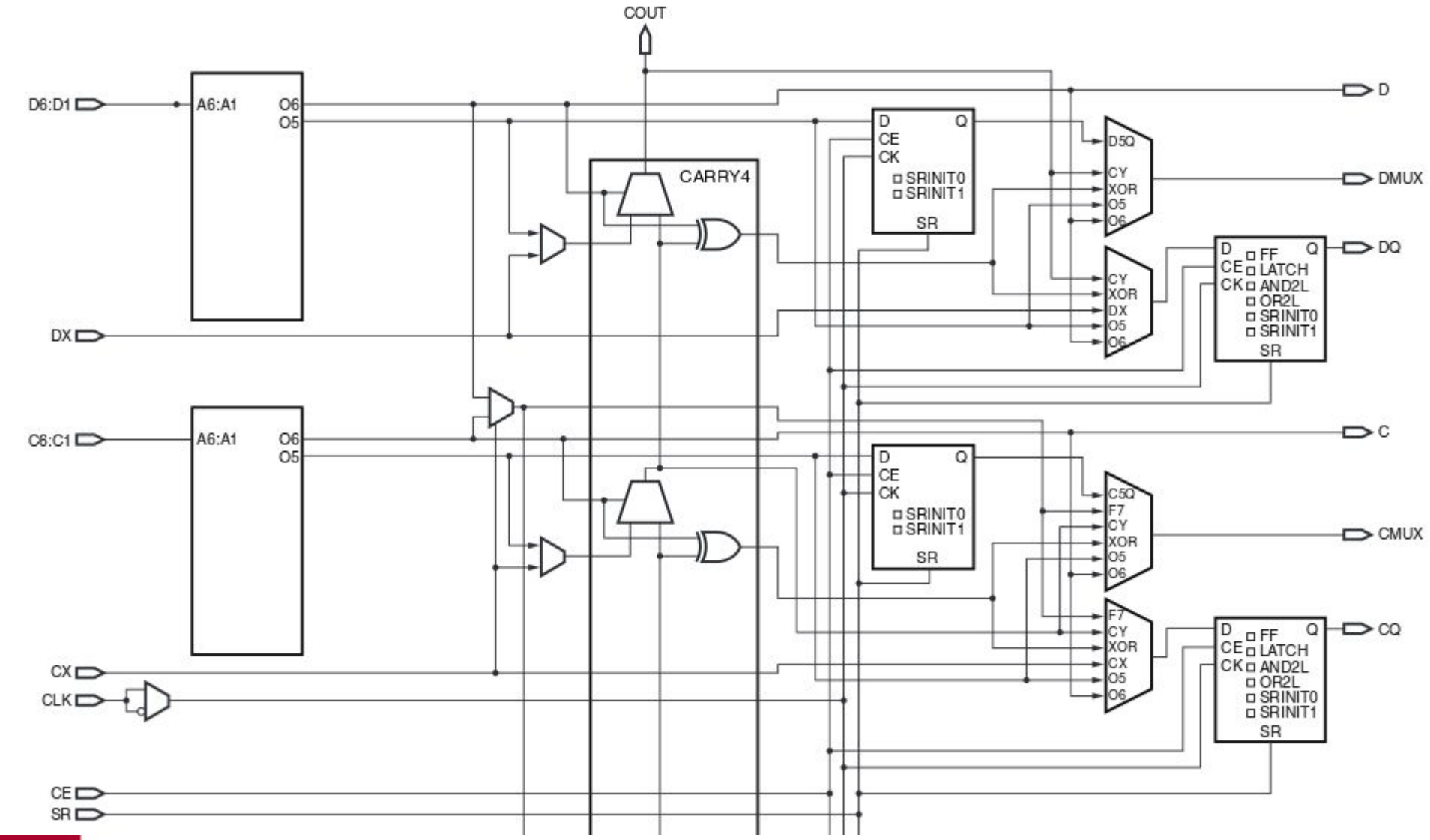
- K * N-input LUT (LUT = Look-Up Table)
- K * Flip-flops (which are also configurable)

K = 2 in old technologies, 4+ in modern technologies

N also increases in modern technologies (6 in Spartan-6)

Xilinx typically organizes CLB in ‘Slices’

½ Slice Spartan-6 (= ¼ CLB)



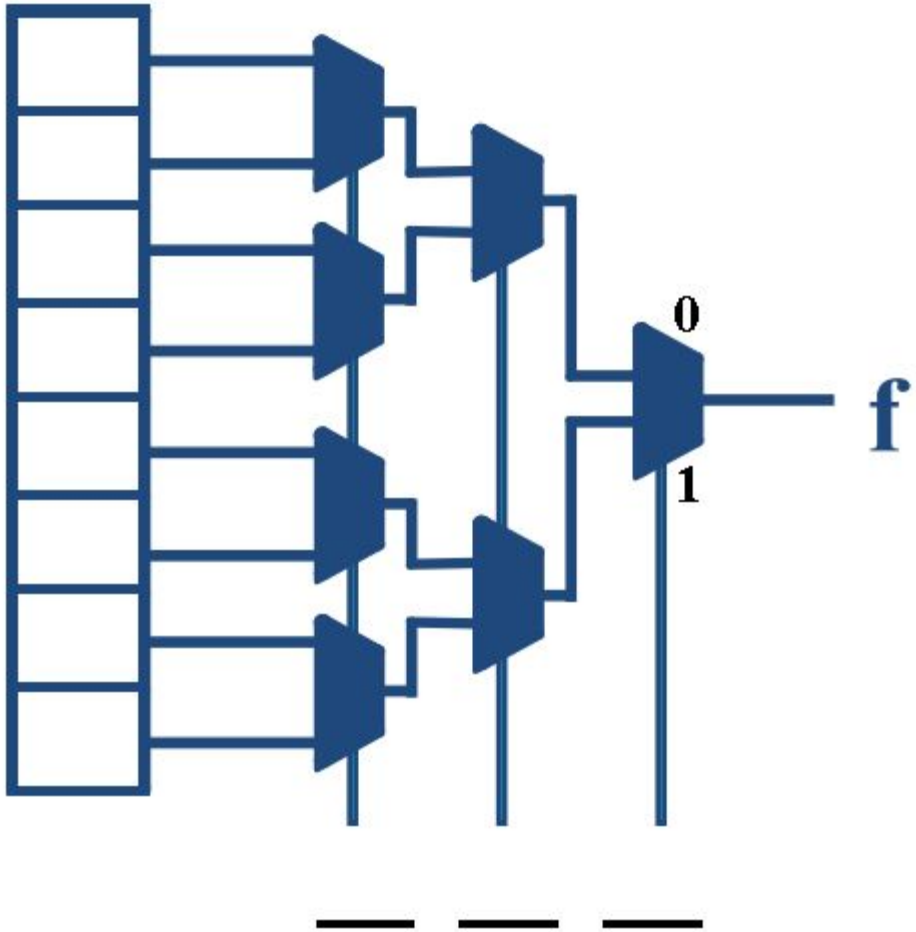
Look-Up Tables (LUTs)

Instead of implement logic functions with logic gates, in FPGA they are implemented with truth tables

- e.g.: A 4-input LUT (‘4-LUT’) can implement any 4-input logic function

LUTs

SRAM



3-LUT

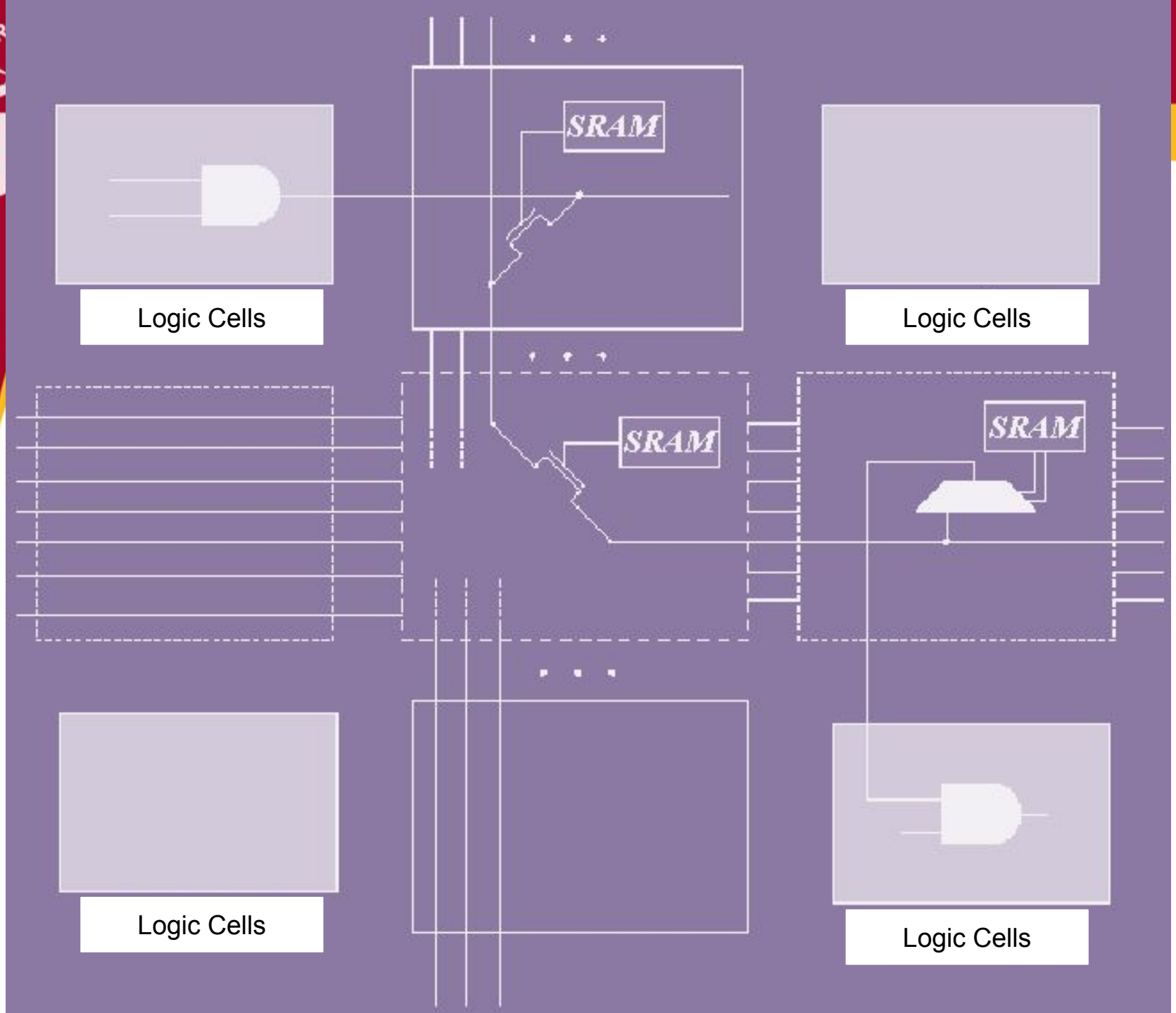
Exercise

Configure the LUT so it implements the function

$F = ABC + A\overline{B}\overline{C}$

Routing resources

- PIP: Programmable Interconnection Points
- Long and short lines (connections)
- Dedicated resources for clock (e.g.: BUFG)


SRAM
Logic Cells
Logic Cells
SRAM
SRAM
Logic Cells
Logic Cells

Configurability and Reconfigurability

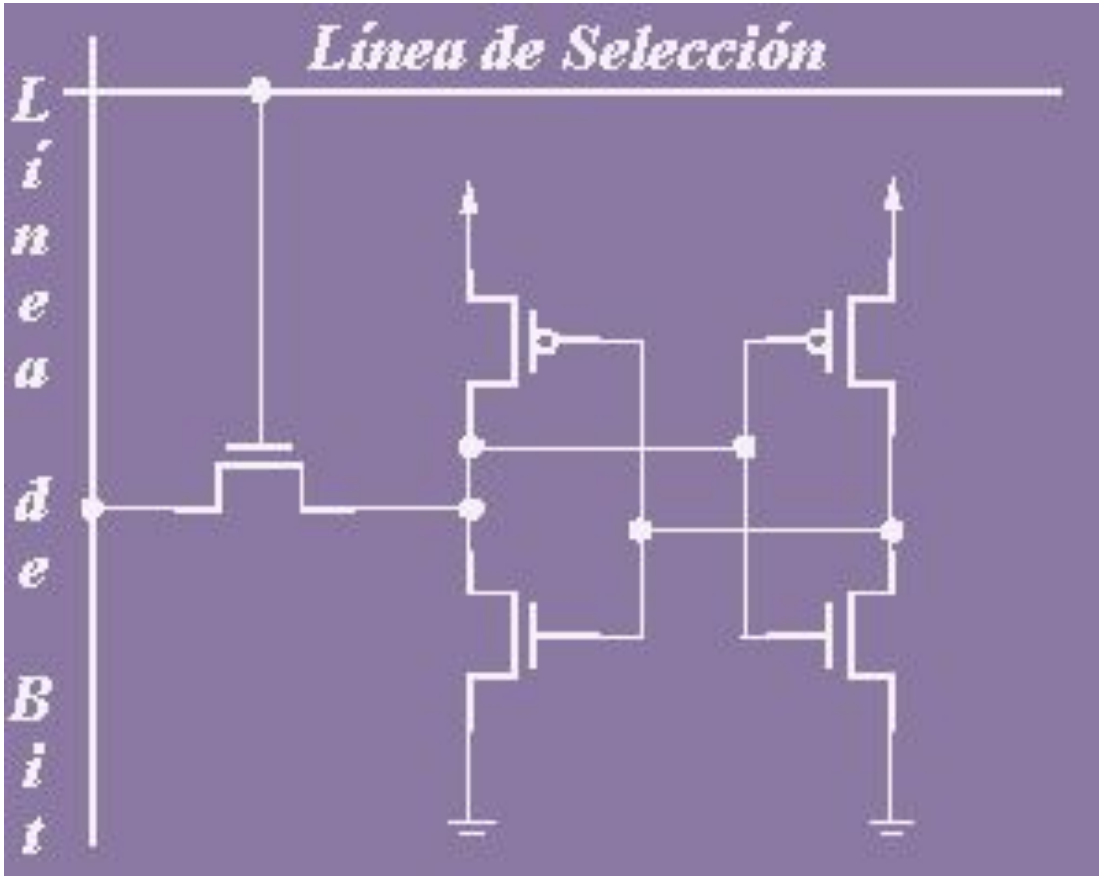
There are three technologies:

- SRAM: reconfigurable, volatile, very widespread, leverages the standard CMOS process
- Flash: reconfigurable, non-volatile, non-standard fabrication process
- Antifuse: non-reconfigurable, non-standard fabrication process

SRAM cell

Two inverters in feedback configuration

4 transistors, but standard CMOS



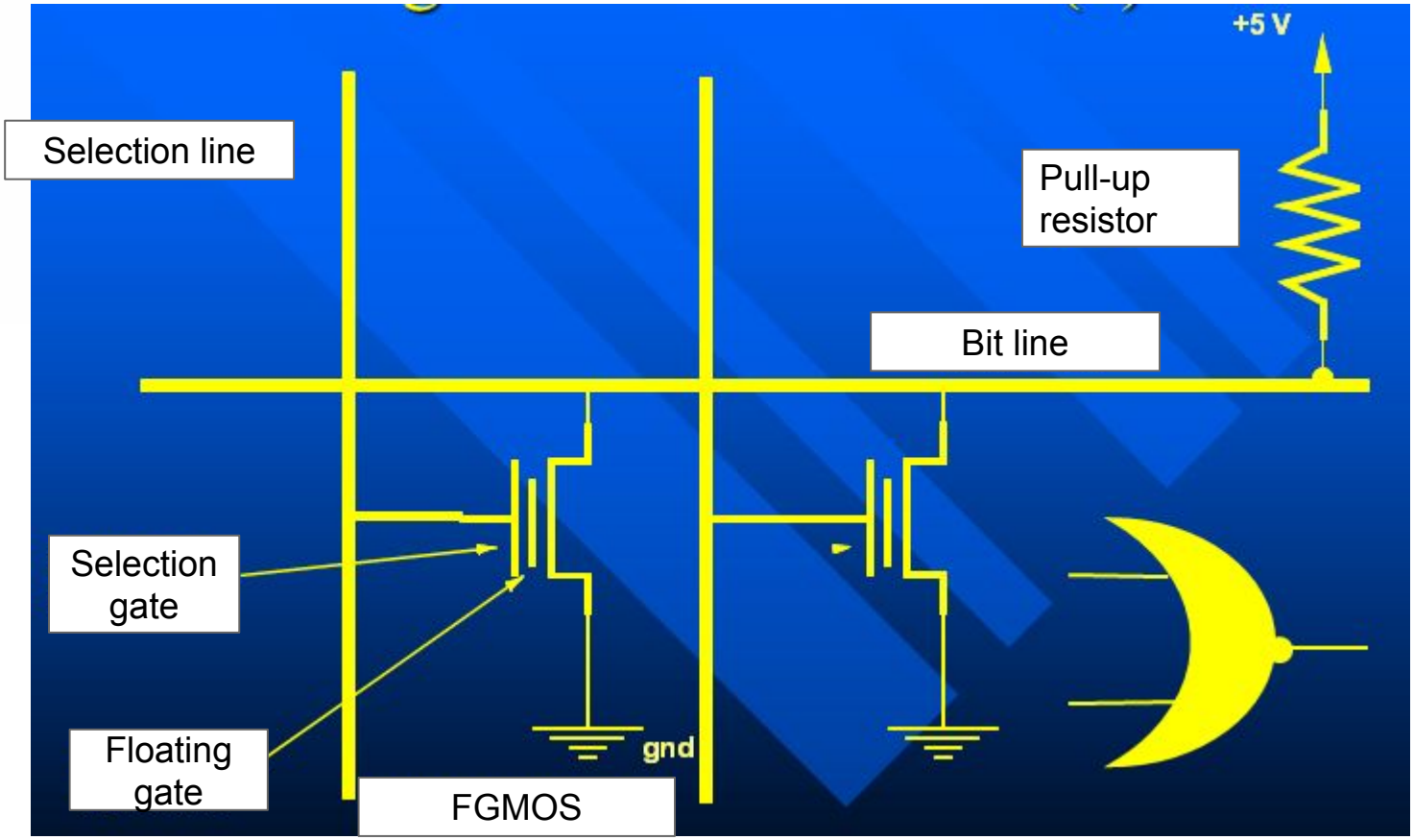
Flash technologies

They are based on the use of FGMOS (Floating-Gate MOS) transistors

- So they require technologies with 2 levels of polysilicon

If the floating gate is charged:
-> Threshold voltage (Vt) increases
-> The transistor cannot be seitched on even with Vdd on its gate

Example of Flash configurability



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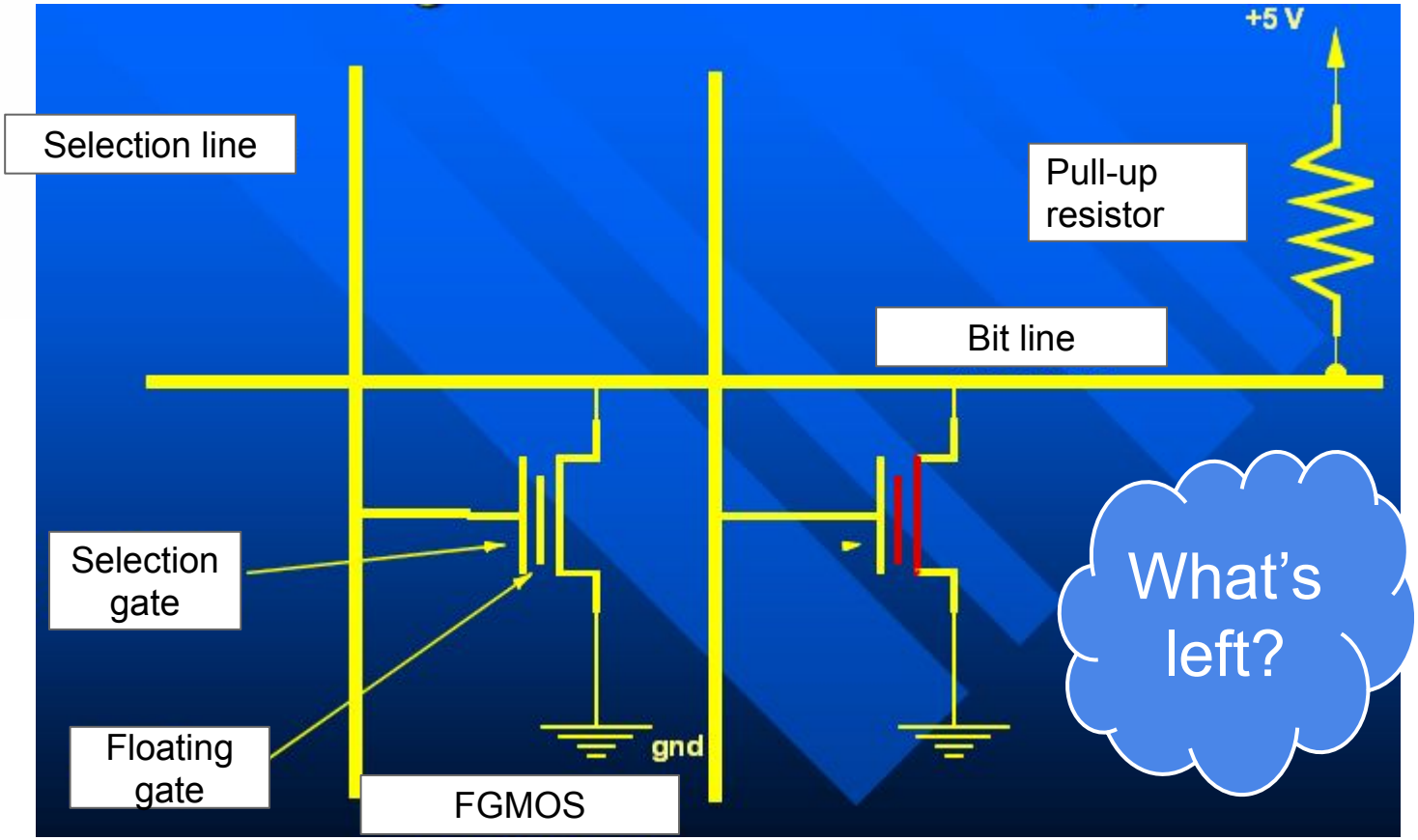

Antifuse technologies

- OTP: One Time Programmable
- Require a specific process (non-standard CMOS)