Advanced Digital Systems and Applications

Academic Year 2025-2026

Syllabus contents
Advanced Programmable Logic Systems

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Taught both in English and Spanish

- Group 1: Spanish
- **Group 2: English**

Theory lessons

- 18-November (G1), **17-November (G2)**
- 2-December (G1), **1-December (G2)**
- 9-December (G1), **15-December (G2)**

- 13-January (G1), **12-January (G2)** (beginning of the lessons): Continuous evaluation exam (theory)

3 theory lessons of 2h50min each

Lab lessons

3 groups:

- 2 during our assigned class schedule (g1, g2)
- 1 in a different schedule (g3)

- Práctica 1:
  - 16 December (g1)
  - **12 January (after the exam) (g2)**
  - To be determined (g3)
- Práctica 2:
  - 13 January (after the exam) (g1)
  - **To be determined (g2)**
  - To be determined (g3)

Contents: Theory

- FPGA architecture overview
- Methodologies for advanced digital design
- Advanced VHDL
- Verification capabilities for digital electronics

Contents: Lab lessons

- Lab 1: Design of a protocol driver for verification
- Lab 2: Design of a protocol monitor for verification

Software (I)

- For the lab lessons we will use a VHDL simulator
- ISim simulator, included with Xilinx ISE, is old, but good enough for this subject, and occupies much less GBs than Vivado.
  - Can be downloaded from Xilinx's website
  - Webpack license, or 2100@vslicencias4.us.es
  - Doesn't work natively in windows 10, so Xilinx provides a Virtual Machine
    - "Windows 10" download on Xilinx's website is a Linux Virtual Machine with ISE installed

Software (II)

- You really can use any other VHDL simulator, so feel free to choose the one you prefer (Eda Playground, GHDL, Vivado XSim, etc)
- If you are going to use a simulator that is not ISim:
  - Make sure that you have installed it correctly and you know how to use it BEFORE the first lab lesson
  - We won't be able to dedicate time during the lab lessons to help you solve installation problems or usage issues
  - Of course, we can help you during office hourse both before and after the lab lessons
- If it is the first time you use VHDL, ISE is slightly more recommended (due to the availability of review material for it)

‘Particularity’ of the subject

- In this subject we have both students with previous experience with VHDL and students that don’t know anything about it
- But we have to teach something new
  - We cannot teach basic VHDL design again
- Those of you who don’t know VHDL, you have to brush up on the language
  - You have review material on the EV (Enseñanza Virtual) of the subject
  - Any questions, just write me an email!

Review material

- VHDL for synthesis (slides)
- VHDL for synthesis (document)
  - Expanded reference
  - With examples
- Datatypes and the numeric_std package
  - Complements the previous reference
- Xilinx ISE quick guide
  - It also explains how to use the simulator, which we will use in the lab lessons
- **Recording of VHDL + ISE lesson**
  - **Spanish only**

Evaluation criteria

Advanced logic programmable systems is 40% of the full subject

This part = 50% theory + 50% lab lessons

- Theory: evaluated through an exam
  - Test (no penalization) + 2 short essay questions
- Lab lessons: 1 report for both lab lessons
  - What is evaluated: implemented functionalities (minimum functionalities to get a 5/10, enhancements score extra points), quality of presented report, quality and cleanliness of code.
  - Submitted through Blackboard (https://ev.us.es)

Lab report submission date

- Submissions through Blackboard (https://ev.us.es)
- Continuous evaluation:
  - Proposed date: 20th January, 2026 (until 23:59)
  - Last teaching day of first semester
  - Since it is continuous evaluation, they must be submitted during the teaching days of the first semester
- Official exams (convocatorias oficiales):
  - The day of the exam (until 23:59)