FPGAS Avanzadas

Mercado Actual de las FPGAS (seguramente hay que actualizarse)

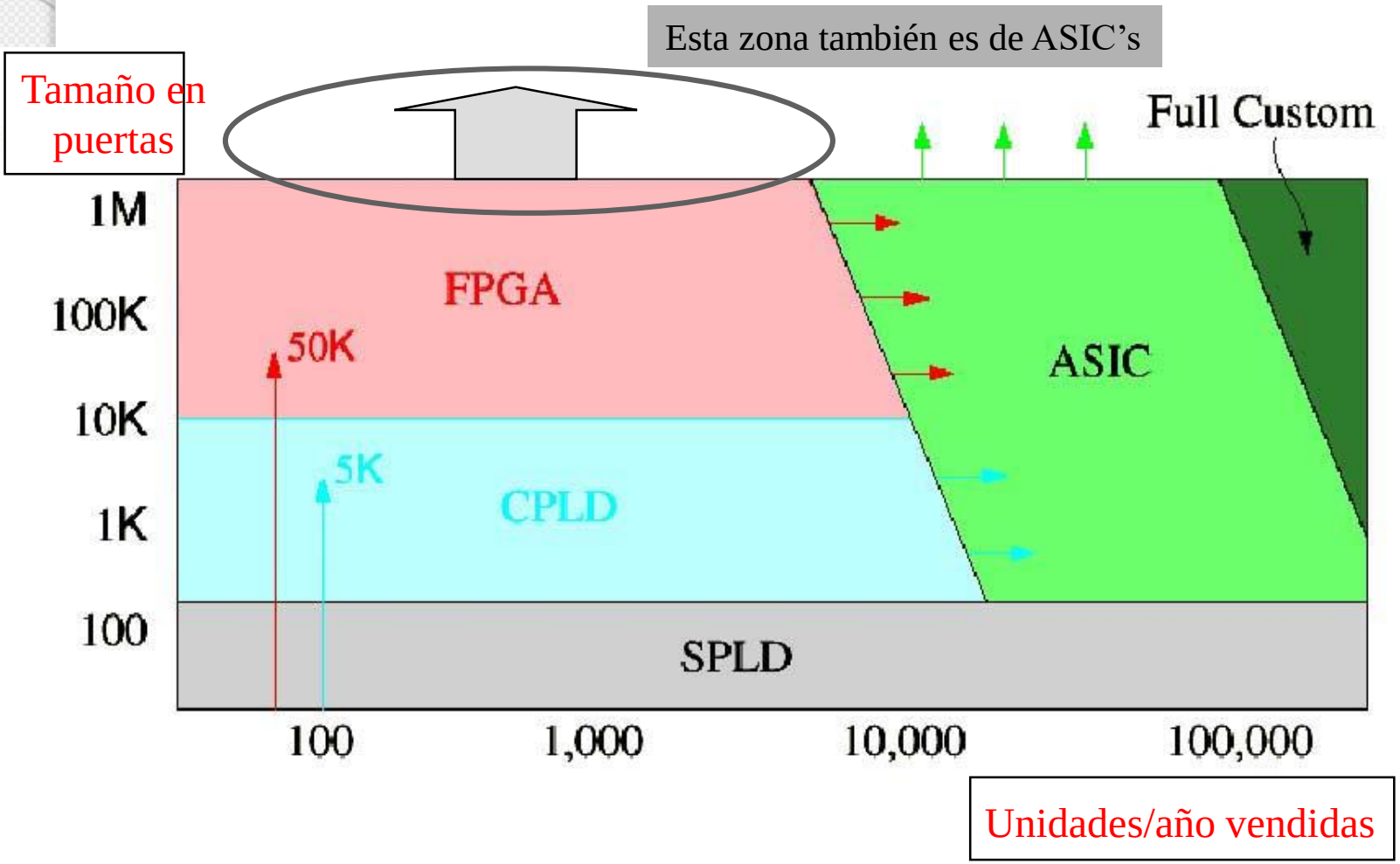
Tema 9

(Darwin era ing. electrónico)

Contenidos:

- Propuestas Actuales de Xilinx
- Propuestas Actuales de Altera
- Propuestas Actuales de Microsemi
- Otras FPGAs del mercado
- Apéndice A. FPGAs Rad-tolerant

Mercado de las nuevas FPGA's



Nuevas prestaciones

- FPGA convencional: hasta 40MHz, a 5V
- FPGA avanzada: 400Mhz
  - Canales de rutado especiales que compensan los posibles *skews* del reloj
  - Para poder trabajar a estas frecuencias se baja la tensión de alimentación:
    - 3,3V
    - 2,5V 1,25V 1,18V 1,0V
    - 0,9V

Capacidad disponible

- Puertas lógicas disponibles: 8M
- Memoria interna configurable: 100Kbit
- Entradas/salidas configurables:
  - 800 dependiendo del encapsulado
  - Compatible con un buen número de familias lógicas
- Estándar IEEE Std.1149.1 (JTAG)

Mecanismos de Programación

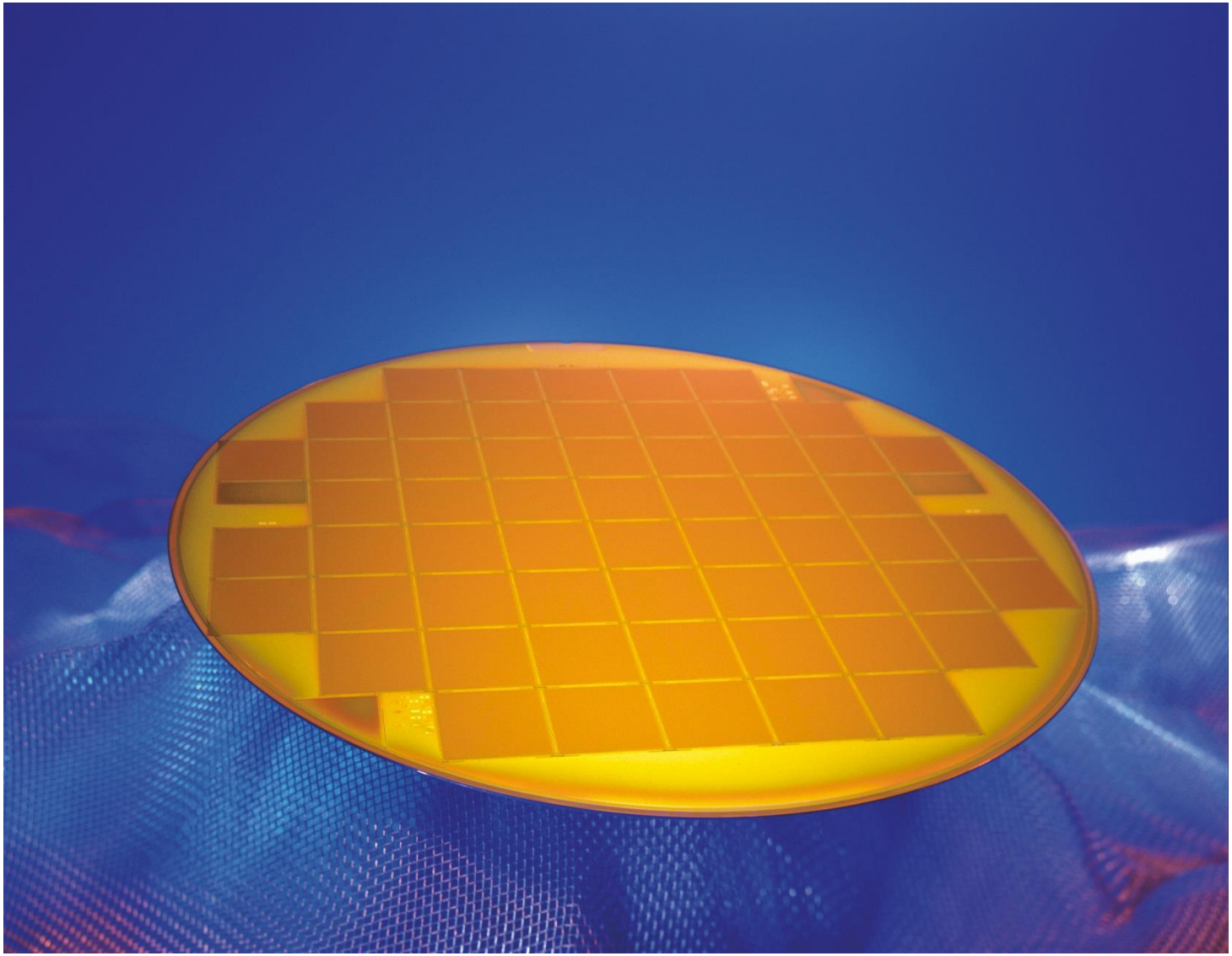
- Tecnología SRAM reprogramable y memorias de interruptores FLASH (no volátil)
- Botado desde PROM's (no flash) o desde un host. Permiten reconfiguración parcial.
- Eliminan los programadores específicos de las FPGA's menores.

TECONOLOGÍAS

- CMOS Convencional (SRAM).
- 0.13μm, 90nm, 65 nm y 8 a 13 más metales
- Conexiones en Cobre

- FLASH (EEPROM)

Oblea de una FPGA



XILINX

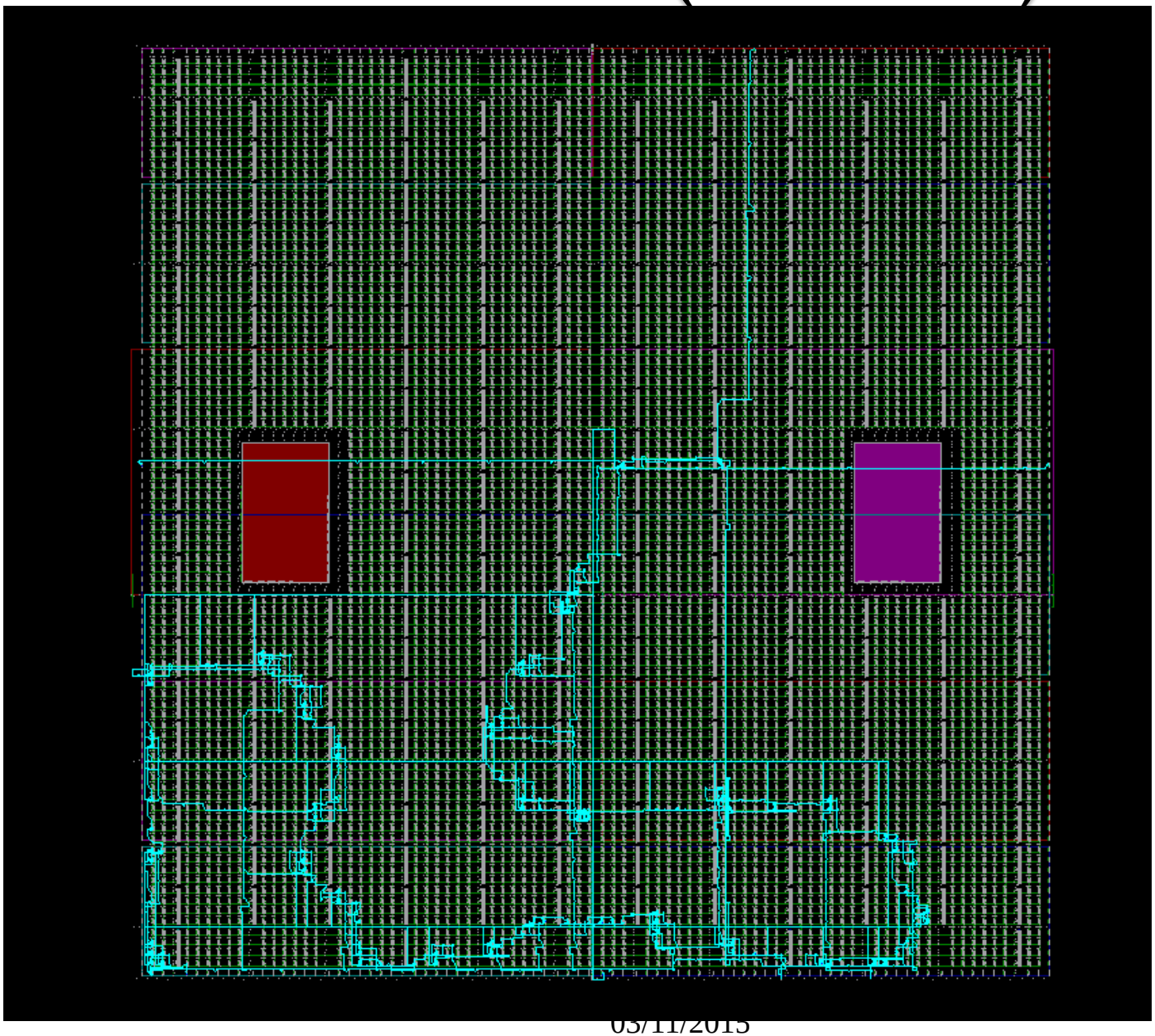
Ha mantenido tecnologías SRAM en toda su gama de productos:

- ☹Sistema con programación volátil
- ☹Baja eficiencia área activa/área utilizada:
  - 💣Precisa 6 transistores/punto de programación
  - 💣Grano grueso (LUT+FF)
- 😐Velocidad de reloj hasta 40Mhz
- ☺Permite la reprogramabilidad
- ☺CMOS Estándar:
  - 🔔No depende de un fabricante
  - 🔔Precios competitivos
- ☺Se ha beneficiado mucho de las tecnologías de alta densidad (nanotecnologías+varias capas de metal)

Oferta Tecnológica de Xilinx

	Serie Avanzada	Serie comercial
Alta Capacidad	Virtex-7 Ultrscale	Spartan 6 Artix-7
Especializada	Artix/Kinetix-7	
CPLD	Coolrunner-II	Coolrunner-XPLA
FlashCPLD	XC9500CV	XC9500XL
Aerospacial	Virtex-5 QV	

Serie Virtex II-Pro (año 2003)

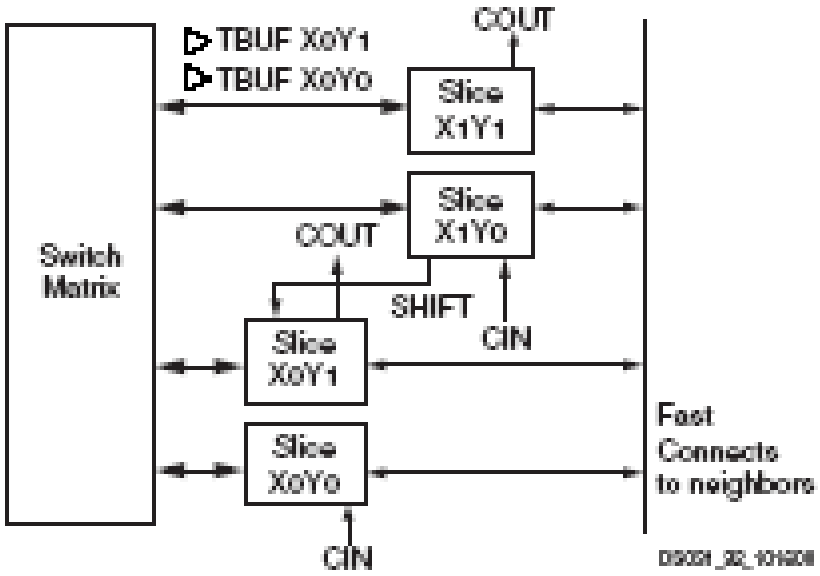


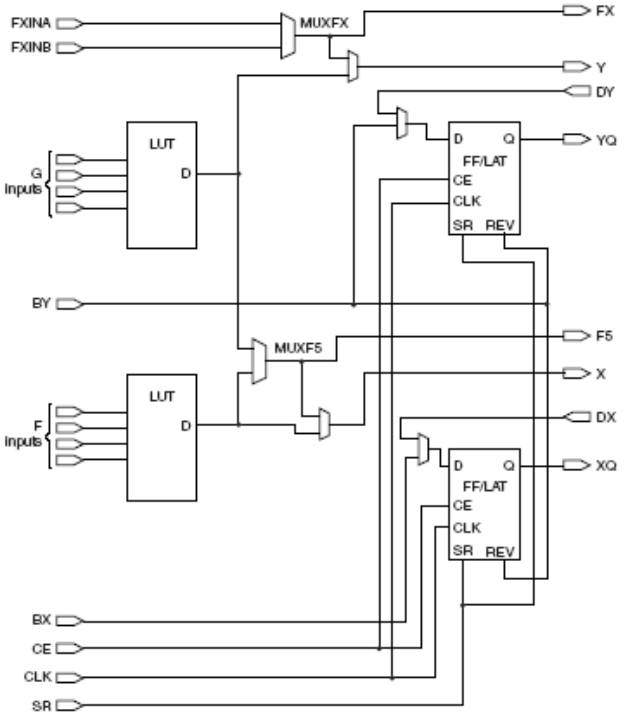
Serie VIRTEX-5

Summary of Virtex-5 Features

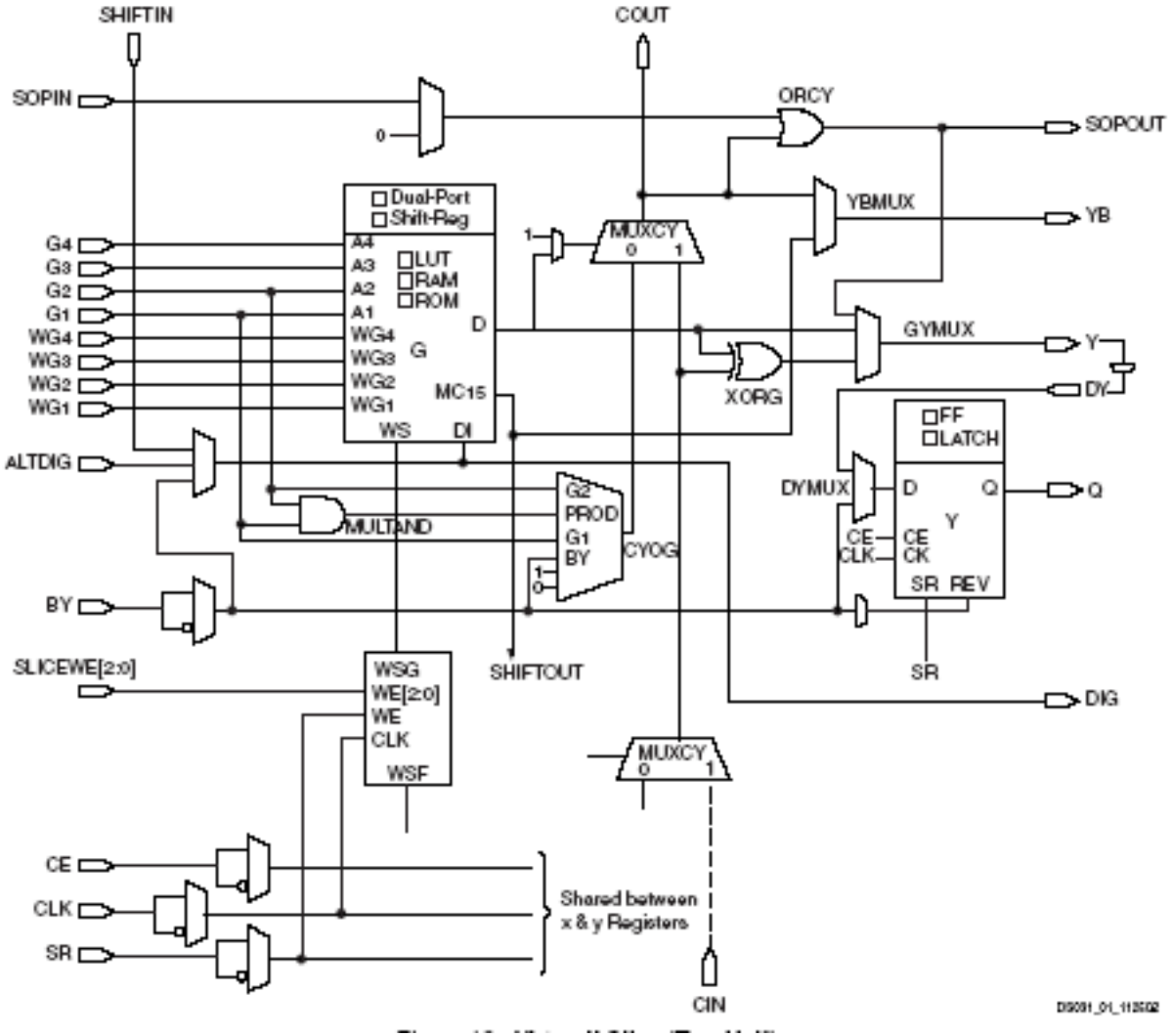
- Four platforms LX, LXT, SXT, and FXT
  - Virtex-5 LX: High-performance general logic applications
  - Virtex-5 LXT: High-performance logic with advanced serial connectivity
  - Virtex-5 SXT: High-performance signal processing applications with advanced serial connectivity
  - Virtex-5 FXT: High-performance embedded systems with advanced serial connectivity
- Cross-platform compatibility
  - LXT, SXT, and FXT devices are footprint compatible in the same package using adjustable voltage regulators
- Most advanced, high-performance, optimal-utilization, FPGA fabric
  - Real 6-input look-up table (LUT) technology
  - Dual 5-LUT option
  - Improved reduced-hop routing
  - 64-bit distributed RAM option
  - SRL32/Dual SRL16 option
- Powerful clock management tile (CMT) clocking
  - Digital Clock Manager (DCM) blocks for zero delay buffering, frequency synthesis, and clock phase shifting
  - PLL blocks for input jitter filtering, zero delay buffering, frequency synthesis, and phase-matched clock division
- 36-Kbit block RAM/FIFOs
  - True dual-port RAM blocks
  - Enhanced optional programmable FIFO logic
  - Programmable
    - True dual-port widths up to x36
    - Simple dual-port widths up to x72
  - Built-in optional error-correction circuitry
  - Optionally program each block as two independent 18-Kbit blocks
- High-performance parallel SelectIO technology
  - 1.2 to 3.3V I/O Operation
  - Source-synchronous interfacing using ChipSync™ technology
  - Digitally-controlled impedance (DCI) active termination
  - Flexible fine-grained I/O banking
  - High-speed memory interface support
- Advanced DSP48E slices
  - 25 x 18, two's complement, multiplication
  - Optional adder, subtracter, and accumulator
  - Optional pipelining
  - Optional bitwise logical functionality
  - Dedicated cascade connections
- Flexible configuration options
  - SPI and Parallel FLASH interface
  - Multi-bitstream support with dedicated fallback reconfiguration logic
  - Auto bus width detection capability
- System Monitoring capability on all devices
  - On-chip/Off-chip thermal monitoring
  - On-chip/Off-chip power supply monitoring
  - JTAG access to all monitored quantities
- Integrated Endpoint blocks for PCI Express
  - LXT, SXT, and FXT Platforms
  - Compliant with the PCI Express Base Specification 1.1
  - x1, x4, or x8 lane support per block
  - Works in conjunction with RocketIO™ transceivers
- Tri-mode 10/100/1000 Mb/s Ethernet MACs
  - LXT, SXT, and FXT Platforms
  - RocketIO transceivers can be used as PHY or connect to external PHY using many soft MII (Media Independent Interface) options
- RocketIO™ GTP transceivers 100 Mb/s to 3.75 Gb/s
  - LXT and SXT Platforms
- RocketIO GTX transceivers 750 Mb/s to 6.5 Gb/s
  - FXT Platform only
- PowerPC 440 Microprocessors
  - FXT Platform only
  - RISC architecture
  - 7-stage pipeline
  - 32-Kbyte instruction and data caches included
  - Optimized processor interface structure (crossbar)
- 65-nm copper CMOS process technology
- 1.0V core voltage
- High signal-integrity flip-chip packaging available in standard or Pb-free package options

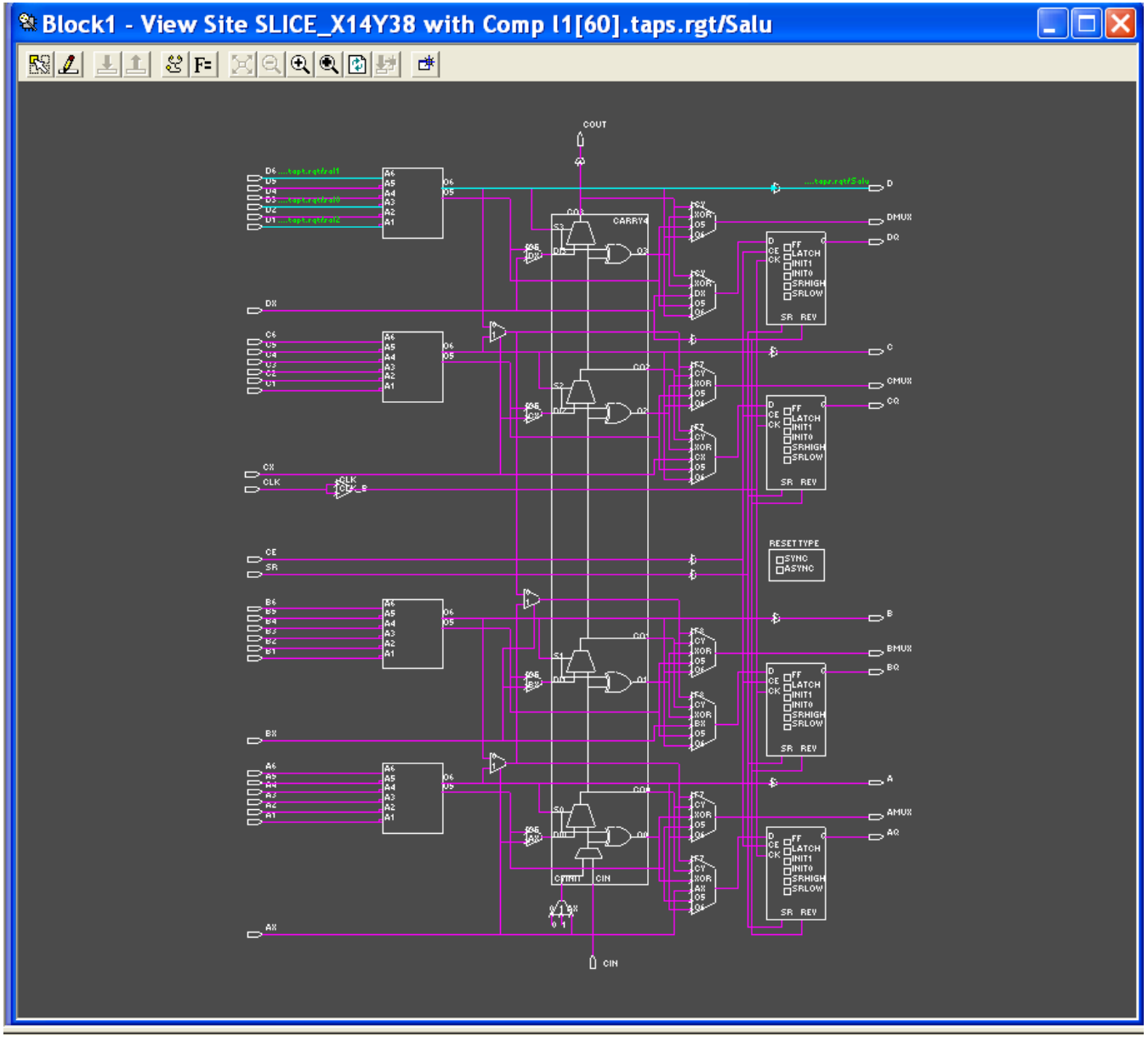
Bloque lógico de VIRTEX-II



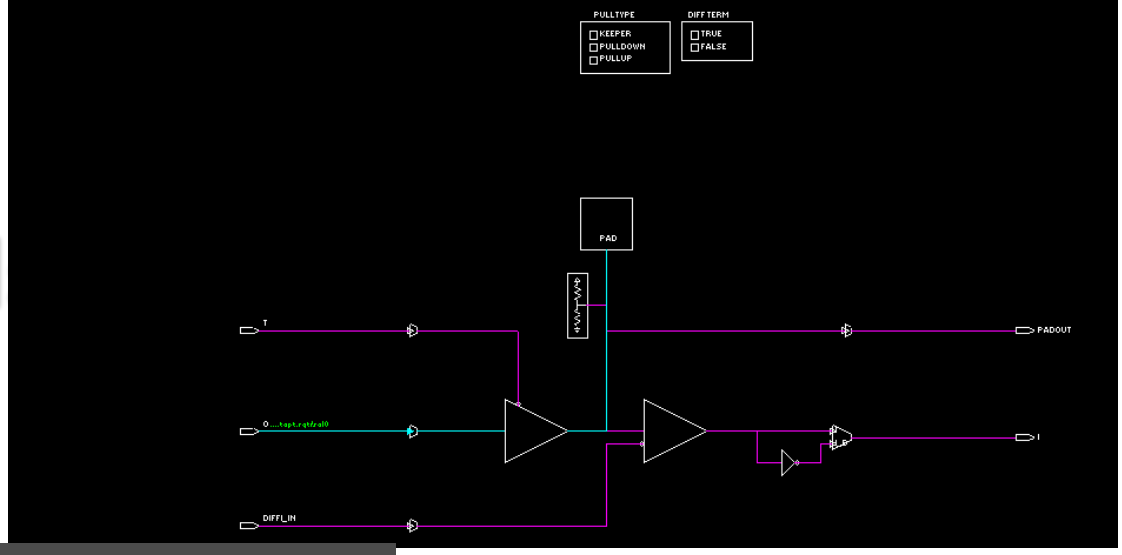


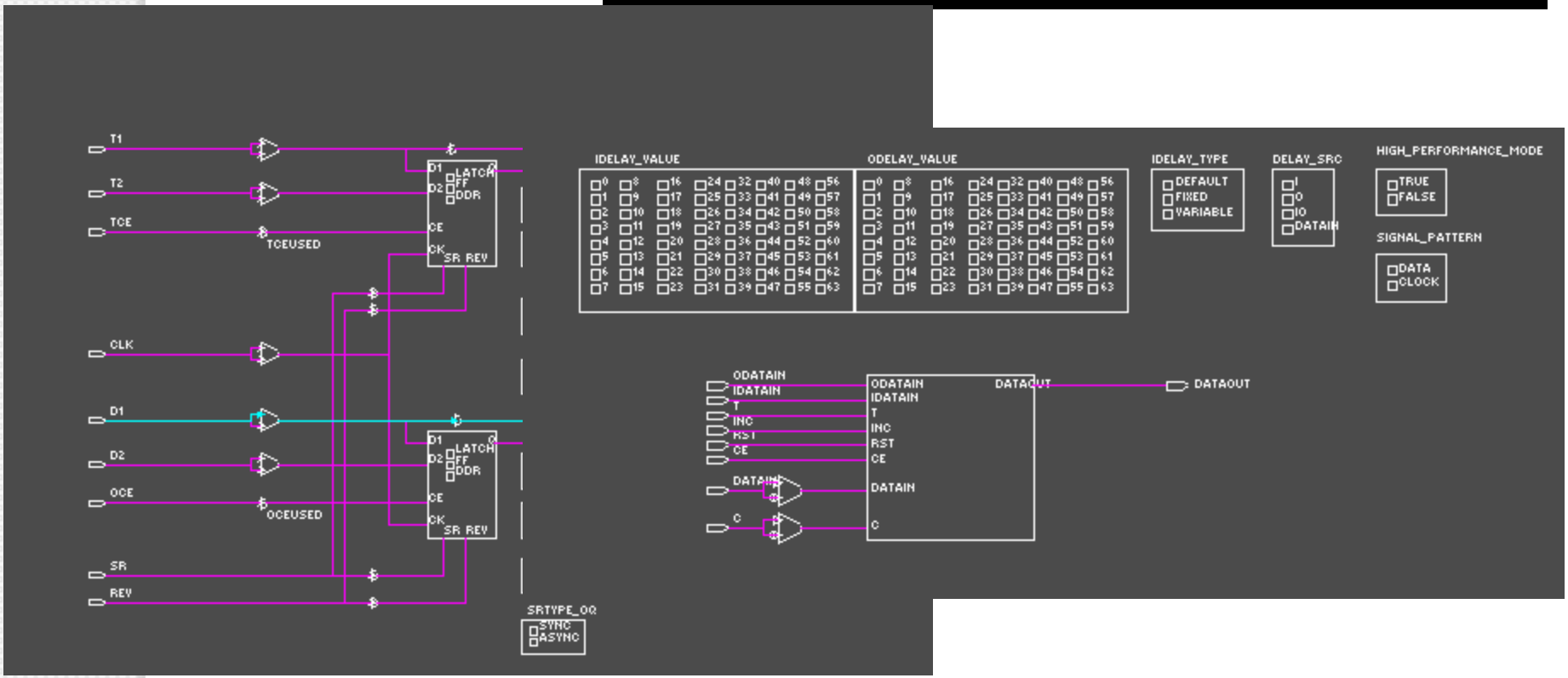
Bloque lógico elemental




Block1 - View Site SLICE_X14Y38 with Comp I1[60].taps.rgt/Salu
COUT
CARRY4
D
DMUX
DQ
C
CMUX
CQ
B
BMUX
BQ
A
AMUX
AQ
DX
CX
CLK
CE
SR
BX
AX
CIN
RESETTYPE
SYNC
ASYNC
FF
LATCH
SR_REV

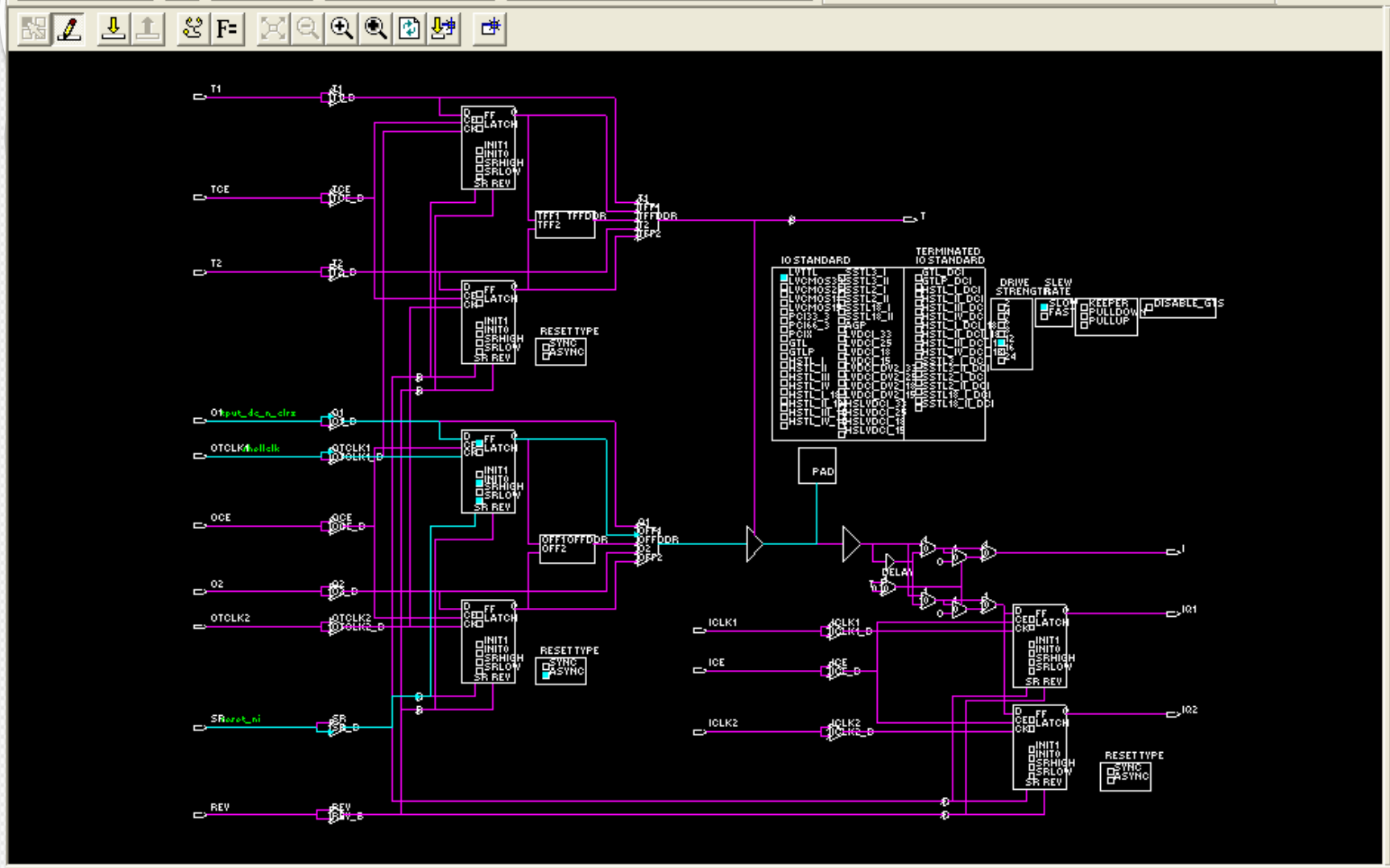
Bloque de entrad salida





Xilinx FPGA Editor - ftunshades_top.ncd - [Block1 - Edit Comp dispclrz at Site D6]

File Edit View Tools Window Help



exit
add
attrib
autoroute
clear
delay
delete
drc
editblock
editmode
find
yellow
hilite
ila
info
probes
autoprobe
route
route -fanout
swap
unroute

```
comp "dispclrz",  site "D6",  bonded type = IOB,  pad name = PAD301,  pin name = D6  (RPM grid X303Y455)
```

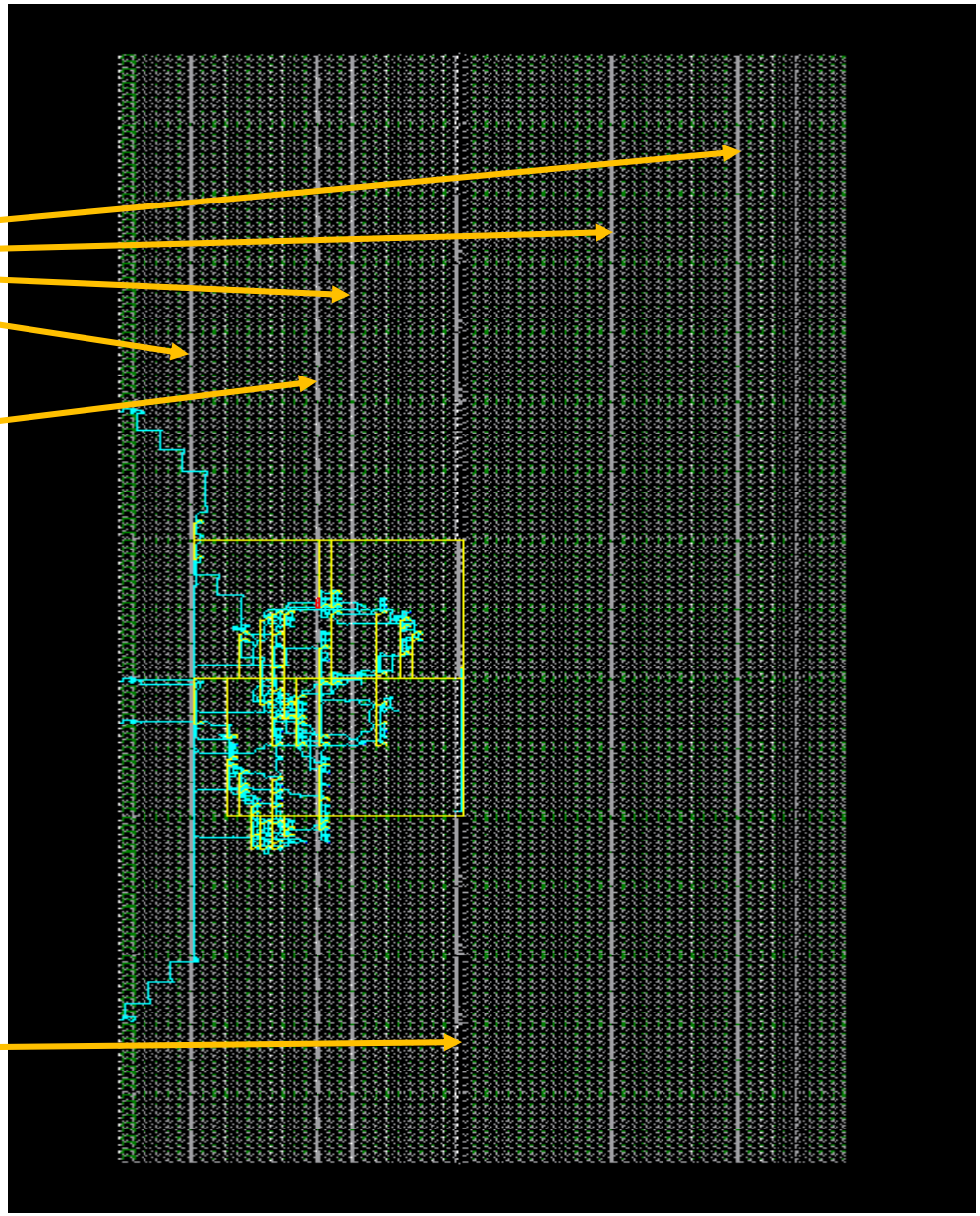
For Help, press F1

xc2v8000-4ff1152 Read Write

Bloques de SRAM

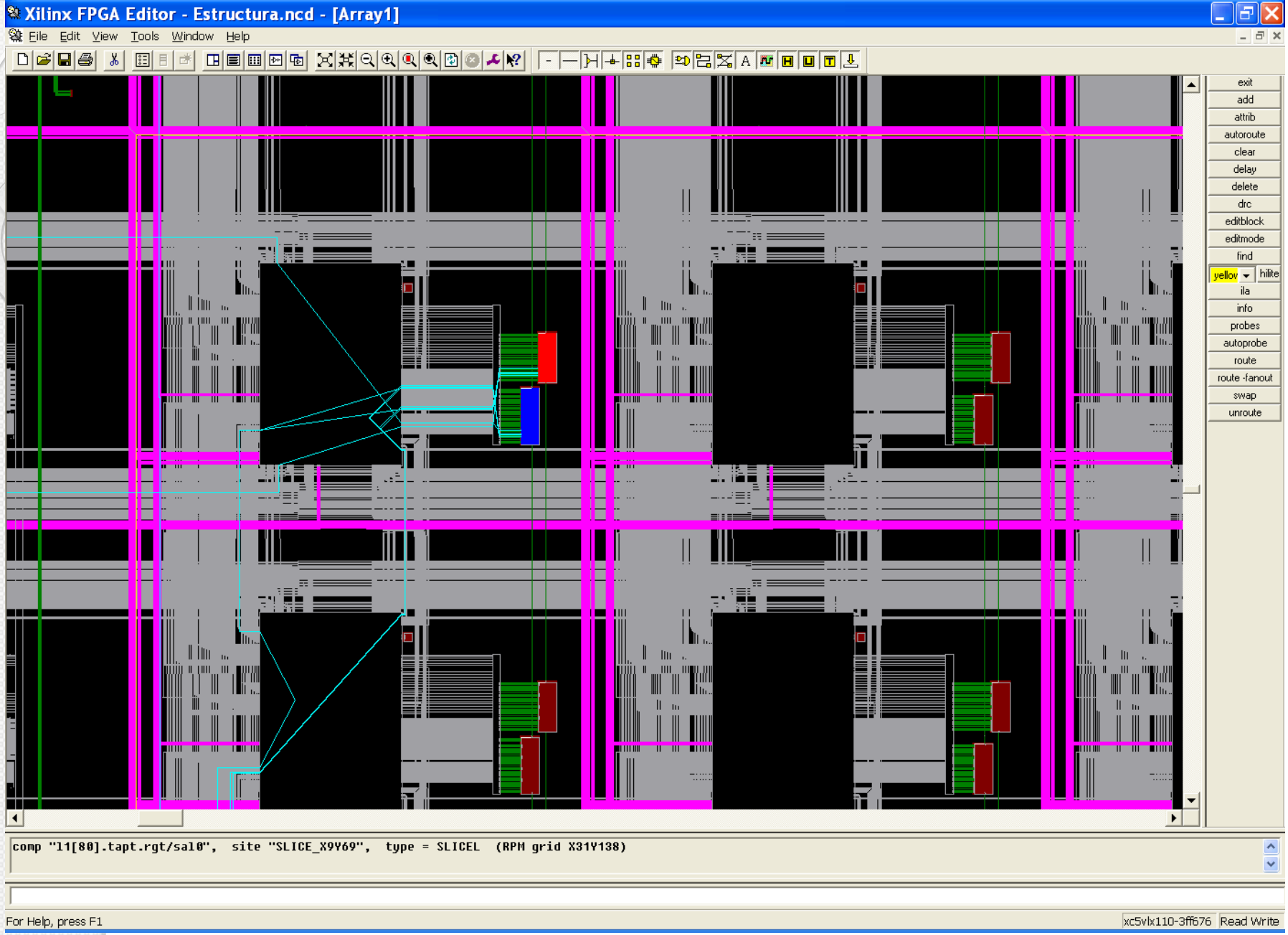
Bloques DSP

Generadores de Reloj

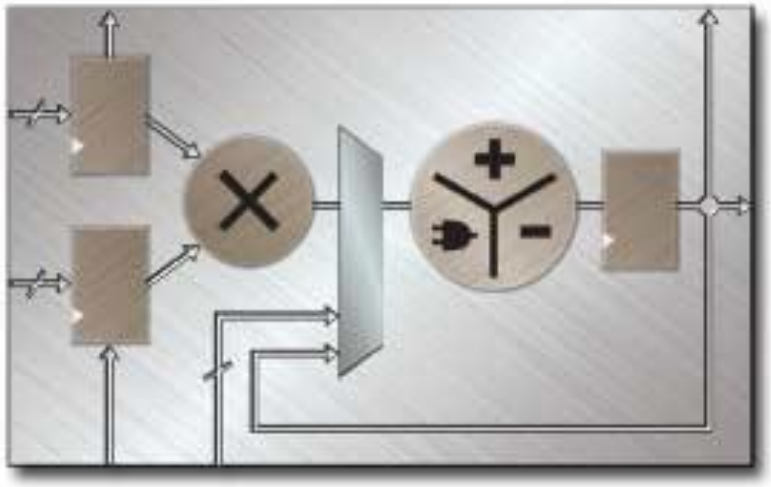


Estructura de Rutado

- Nivel de jerarquía local:
  - Conexionado en las 4 direcciones con las CLB's adyacentes
  - Realimentaciones internas en la CLB
- Nivel de jerarquia global:
  - 24 Segmentos de alcance 1 CLB
  - 96 Segmentos de alcance 6 CLB's
  - 12 Segmentos de alcance máximo bidireccionales, tanto en vertical como en horizontal
- Especiales:
  - Buses triestado horizontales y seccionables (4 líneas)
  - Carry rápido en vertical


Xilinx FPGA Editor - Estructura.ncd - [Array1]
File Edit View Tools Window Help
exit
add
attrib
autoroute
clear
delay
delete
drc
editblock
editmode
find
yellow
hilite
ila
info
probes
autoprobe
route
route -fanout
swap
unroute
comp "l1[80].tapt.rgt/sal0", site "SLICE_X9Y69", type = SLICEL (RPM grid X31Y138)
For Help, press F1
xc5vlx110-3ff676
Read Write

Virtex-5. Bloque DSP



Virtex 5

		Virtex-5 LX Platform						Virtex-5 LXT Platform				
		LX30	LX50	LX85	LX110	LX220	LX330	LX30T	LX50T	LX85T	LX110T	LX330T
	Part Number	XC5VLX30	XC5VLX50	XC5VLX85	XC5VLX110	XC5VLX220	XC5VLX330	XC5VLX30T	XC5VLX50T	XC5VLX85T	XC5VLX110T	XC5VLX330T
	EasyPath™ Cost Reduction Solutions (1)	—	—	XCE5VLX85	XCE5VLX110	XCE5VLX220	XCE5VLX330	—	—	—	XCE5VLX110T	XCE5VLX330T
CLB Resources	CLB Array Size (Row x Column)	80 x 30	120 x 30	120 x 54	160 x 54	160 x 108	240 x 108	80 x 30	120 x 30	120 x 54	160 x 54	240 x 108
	Slices (2)	4,800	7,200	12,960	17,280	34,560	51,840	4,800	7,200	12,960	17,280	51,840
	Logic Cells (2)	30,720	46,080	82,944	110,592	221,184	331,776	30,720	46,080	82,944	110,592	331,776
	CLB Flip-Flops	19,200	28,800	51,840	69,120	138,240	207,360	19,200	28,800	51,840	69,120	207,360
Memory Resources	Maximum Distributed RAM (kbits)	320	480	840	1,120	2,280	3,420	320	480	840	1,120	3,420
	Block RAM/FIFO w/ECC (36kbits each)	32	48	96	128	192	288	36	60	108	148	324
	Total Block RAM (kbits)	1,152	1,728	3,456	4,608	6,912	10,368	1,296	2,160	3,888	5,328	11,664
Clock Resources	Digital Clock Manager (DCM)	4	12	12	12	12	12	4	12	12	12	12
	Phase Locked Loop (PLL)/PMCD	2	6	6	6	6	6	2	6	6	6	6
I/O Resources	Maximum SelectIO™ Pins	400	560	560	800	800	1,200	360	480	480	680	960
	SelectIO™ Banks	13	17	17	23	23	35	13	17	17	23	35
	Digitally Controlled Impedance	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	Maximum Differential I/O Pairs	200	280	280	400	400	600	180	240	240	340	480
	I/O Standards	HT, LVDS, LVDSEXT, RSDS, BLVDS, ULVDS, LVPECL, LVCMOS33, LVCMOS25, LVCMOS18, LVCMOS15, LVTTL, PCI33, PCI66, PCI-X, GTL, GTL+, HSTL I (1.2V,1.5V,1.8V), HSTL II (1.5V,1.8V), HSTL III (1.5V,1.8V), HSTL IV (1.5V,1.8V), SSTL2 I, SSTL2 II, SSTL18 I, SSTL18 II										
Embedded Hard IP Resources	DSP48E Slices	32	48	48	64	128	192	32	48	48	64	192
	PCI Express Endpoint Blocks	0	0	0	0	0	0	1	1	1	1	1
	10/100/1000 Ethernet MAC Blocks	0	0	0	0	0	0	4	4	4	4	4
	RocketIO™ GTP Low-Power Transceivers	0	0	0	0	0	0	8	12	12	16	24
	Configuration Memory (Mbits)	8.4	12.6	21.8	29.1	53.1	79.7	9.4	14.1	23.3	31.1	82.7
Package (4)	Area	I/O	MGT (5)									
FF324	19 x 19 mm	220		220	220							
FF676	27 x 27 mm	440		400	440	440	440					
FF1153	35 x 35 mm	800			560	560	800					
FF1760	42.5 x 42.5 mm	1200					800	800	1200			
FF665	27 x 27mm	360	8						360 (8)	360 (8)		
FF1136	35 x 35mm	640	16							480 (12)	480 (12)	640 (16)	
FF1738	42.5 x 42.5mm	960	24									680 (16)	960 (24)

Features	Artix-7	Kintex-7	Virtex-7	Spartan-6	Virtex-6
Logic Cells	352,000	480,000	2,000,000	150,000	760,000
BlockRAM	19Mb	34Mb	68Mb	4.8Mb	38Mb
DSP Slices	1,040	1,920	3,600	180	2,016
DSP Performance (symmetric FIR)	1,248GMACS	2,845GMACS	5,335GMACS	140GMACS	2,419GMACS
Transceiver Count	16	32	96	8	72
Transceiver Speed	6.6Gb/s	12.5Gb/s	28.05Gb/s	3.2Gb/s	11.18Gb/s
Total Transceiver Bandwidth (full duplex)	211Gb/s	800Gb/s	2,784Gb/s	50Gb/s	536Gb/s
Memory Interface (DDR3)	1,066Mb/s	1,866Mb/s	1,866Mb/s	800Mb/s	1,066Mb/s
PCI Express® Interface	Gen2x4	Gen2x8	Gen3x8	Gen1x1	Gen2x8
Agile Mixed Signal (AMS)/XADC	Yes	Yes	Yes		Yes
Configuration AES	Yes	Yes	Yes	Yes	Yes
I/O Pins	600	500	1,200	576	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V
EasyPath Cost Reduction Solution	-	Yes	Yes	-	Yes

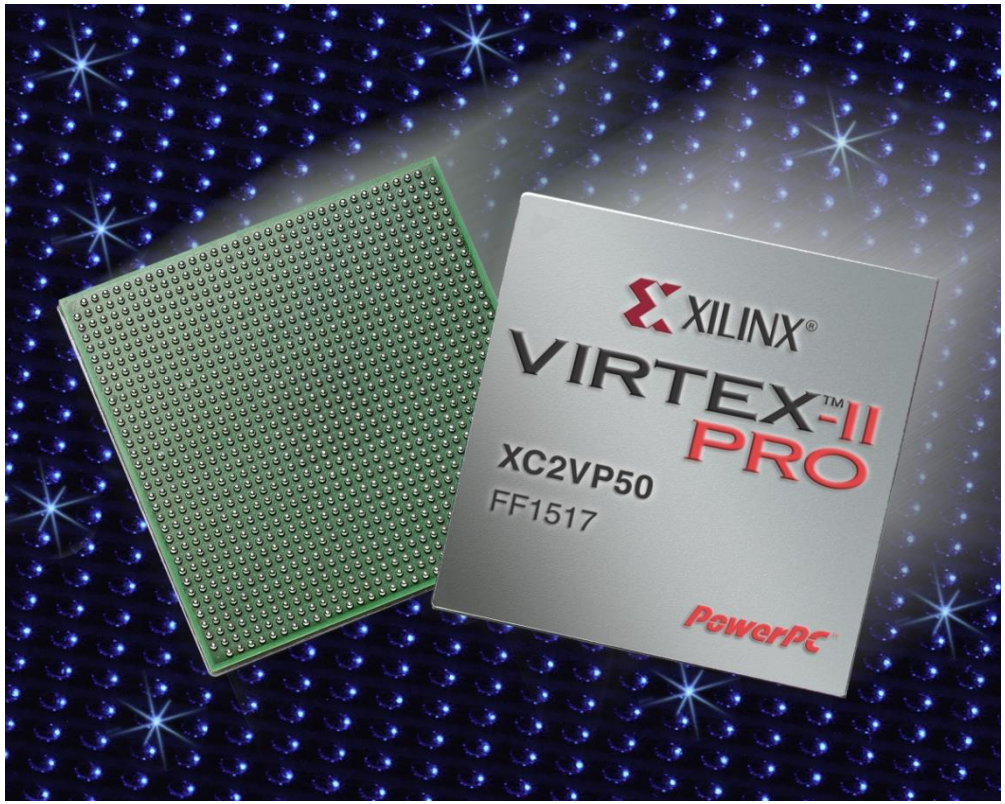
Virtex-7

Maximum Capability	Virtex-7 T Devices	Virtex-7 XT Devices	Virtex-7 HT Devices
Logic density (Logic Cells)	1,955K	1,139K	864K
Peak transceiver speed	12.5Gb/s (GTX)	13.1Gb/s (GTH)	28.05Gb/s (GTZ)
Transceivers	36	96	88
Peak bi-directional serial bandwidth	0.900 Tb/s	2.515Tb/s	2.784Tb/s
DSP throughput (symmetric filter)	2,756 GMACS	5,314 GMACS	5,053 GMACS
Block RAM	46.5Mb	85.0Mb	64.4Mb
PCI Express® interface	Gen2x8	Gen3x8	Gen3x8
I/O pins	1,200	1,100	700

Application	Description
ASIC Prototyping	Build a highly integrated ASIC prototyping solution with the Virtex-7 2000T. With its high logic and processing capacity, mitigate development risks for large ASIC and ASSP designs.
2x100G OTU4 Transponder/Line Card	Build a 2x100G OTU4 Transponder/Line Card using the only 28nm FPGAs that enable designers to integrate two 100G interfaces into a single FPGA for reduced board space, power, and cost.
10GPON/10GEPON OLT Line Card	Meet aggressive 10G port count integration and cost targets for Passive Optical Network (PON) Optical Line Terminal (OLT) Line Cards that bring high-speed networking to the neighborhood/home.
100GE Line Card	Virtex-7 FPGAs offer the right mix of I/O, memory and logic to enable a single-FPGA implementation of new line cards that deliver increased bandwidth.
100G OTN Muxponder	Virtex-7 FPGA XT devices enable a flexible, single-FPGA, 100G OTN Multiplexing Transponder implementation.
300G Interlaken Bridge	Create a 300G Interlaken Bridge that enables infrastructure scaling with devices that deliver up to 1.9Tbps bandwidth for bridging between MAC-NPU, NPU-Switch, NPU-TCAM using the Interlaken industry standard.
400G Line Card	Be first to market with 400GE Line Cards by designing with the only FPGAs to support 400G serial interfaces with next-generation optics.
Portable RADAR Systems	Enable high performance RADAR systems through low power, multi-channel signal recovery and processing.
Terabit Switch Fabric	Virtex-7 FPGA XT device capabilities enable Terabit Switch Fabric to support proliferating 40G/100G ports in networking infrastructure.

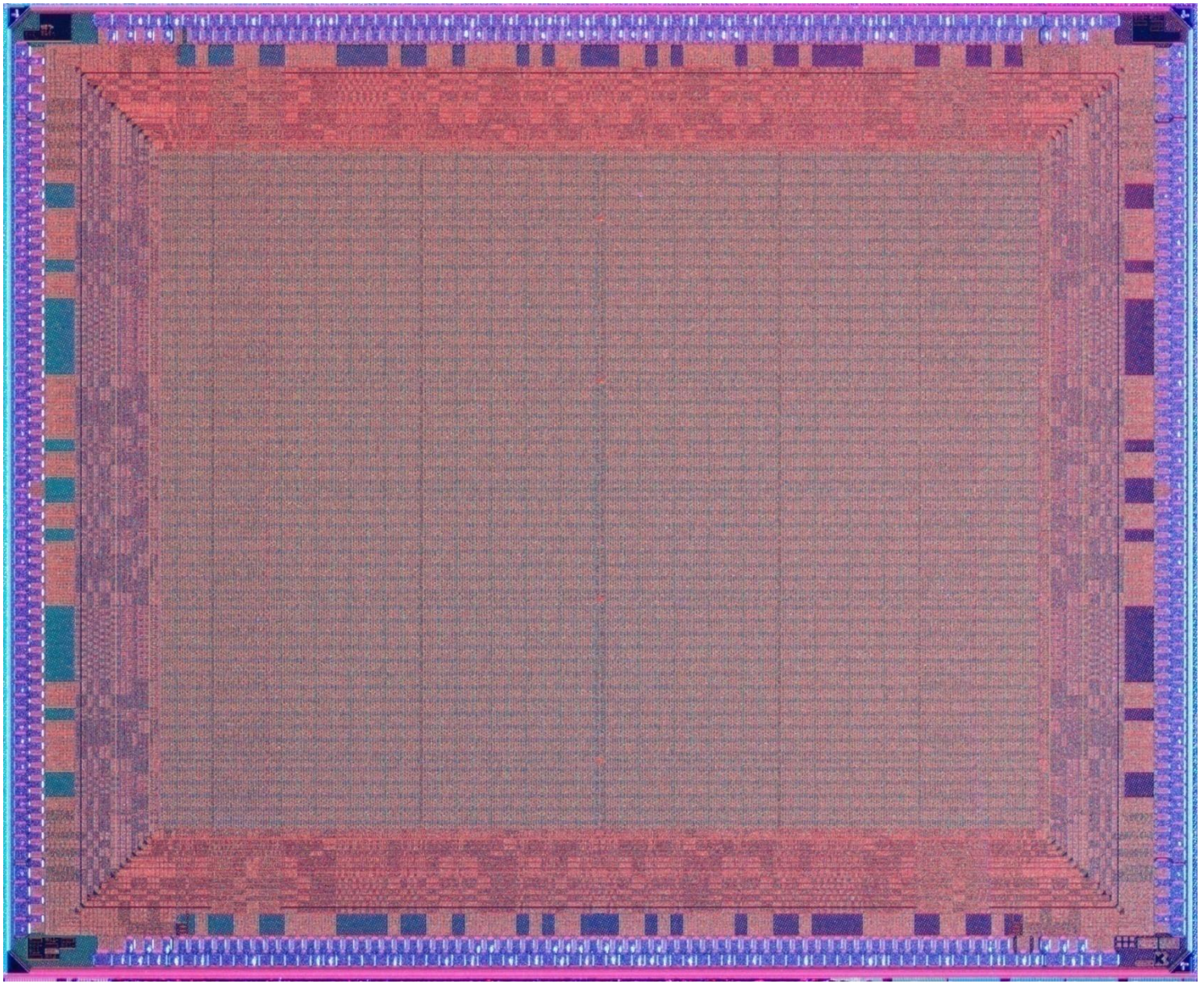
Encapsulados

- Es el problema crítico. Hay que manejar un elevado número de IO's:
  - CS144
  - QFP240
  - BGA560
  - FF1517
- PCB's complejos y con grandes dificultades para soldadura y test



Aplicaciones

- Sustitución de ciertos componentes tradicionalmente reservados a ASIC's:
  - Aplicaciones PCI: 133MHz y 64 bits
  - Equipos de telecomunicación tipo OC3, WiMax,…
  - Estaciones base de satélites
  - Equipos de edición de gráficos, aplicaciones biomédicas
  - Equipos de computación paralela
  - Sistemas HDTV
- Prototipado rápido de sistemas VLSI de Procesamiento digital de señales:
  - IDCT, FFT's, Filtros,...



ALTERA

- FPGA's con estructura tipo CPLD
- Mecanismo de programación tipo EPROM y en serie 10K en SRAM
- Organización jerárquica de los elementos básicos funcionales
- Precisan de un programador propio adaptado a cada modelo de FPGA
- Puertas disponibles: 40.000 en EPROM, hasta 250.000 en SRAM
- Número de IO's: 140

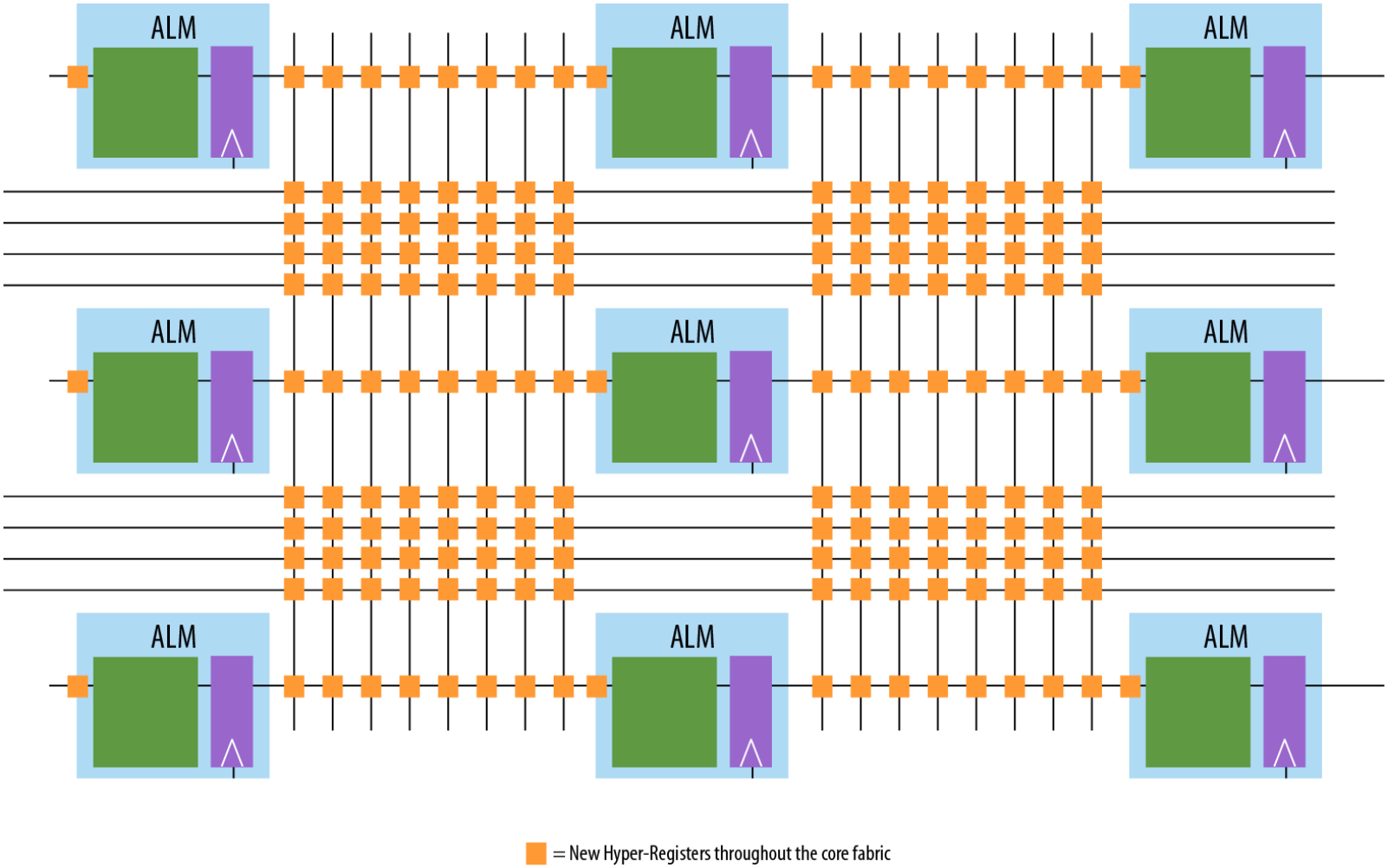
Oferta Tecnológica de ALTERA

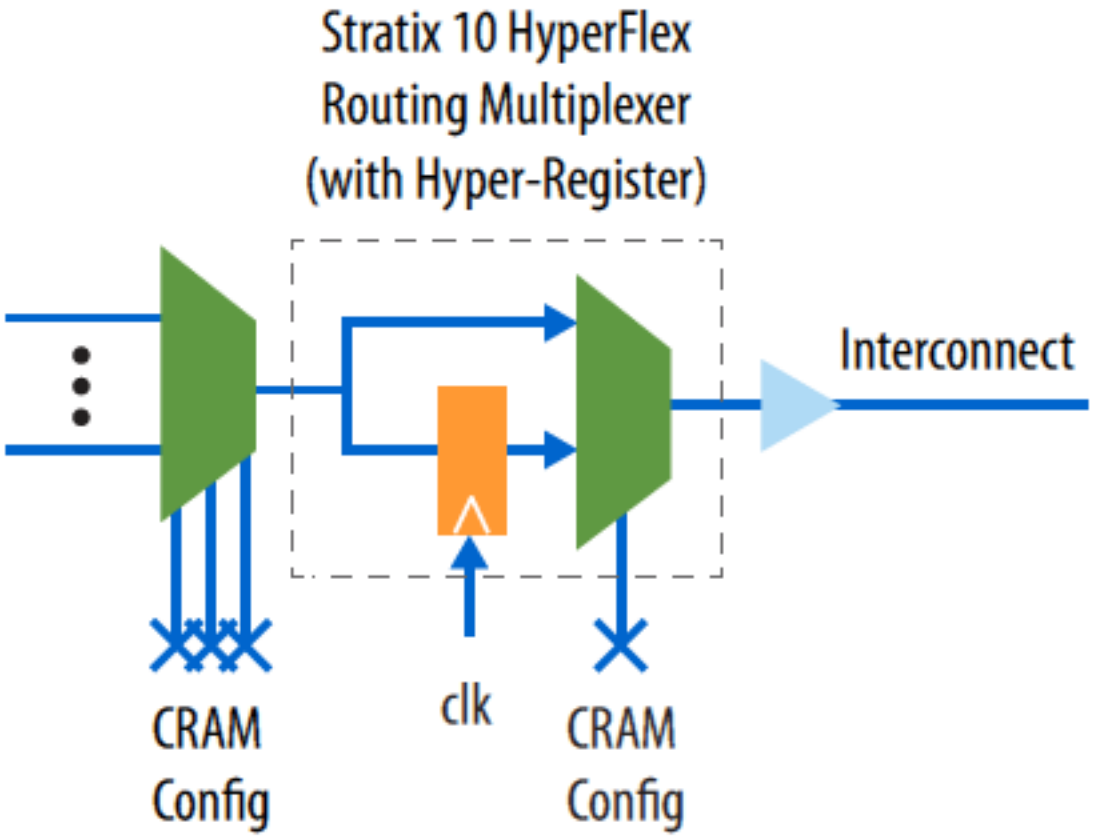
	Serie Avanzada	Serie Comercial
Alta Capacidad	Stratix 10	Cyclone V
Especializada	Arria 10	
CPLD	Max V	
FlashCPLD	Max II	
ASICs	Hardcopy II	Hardcopy

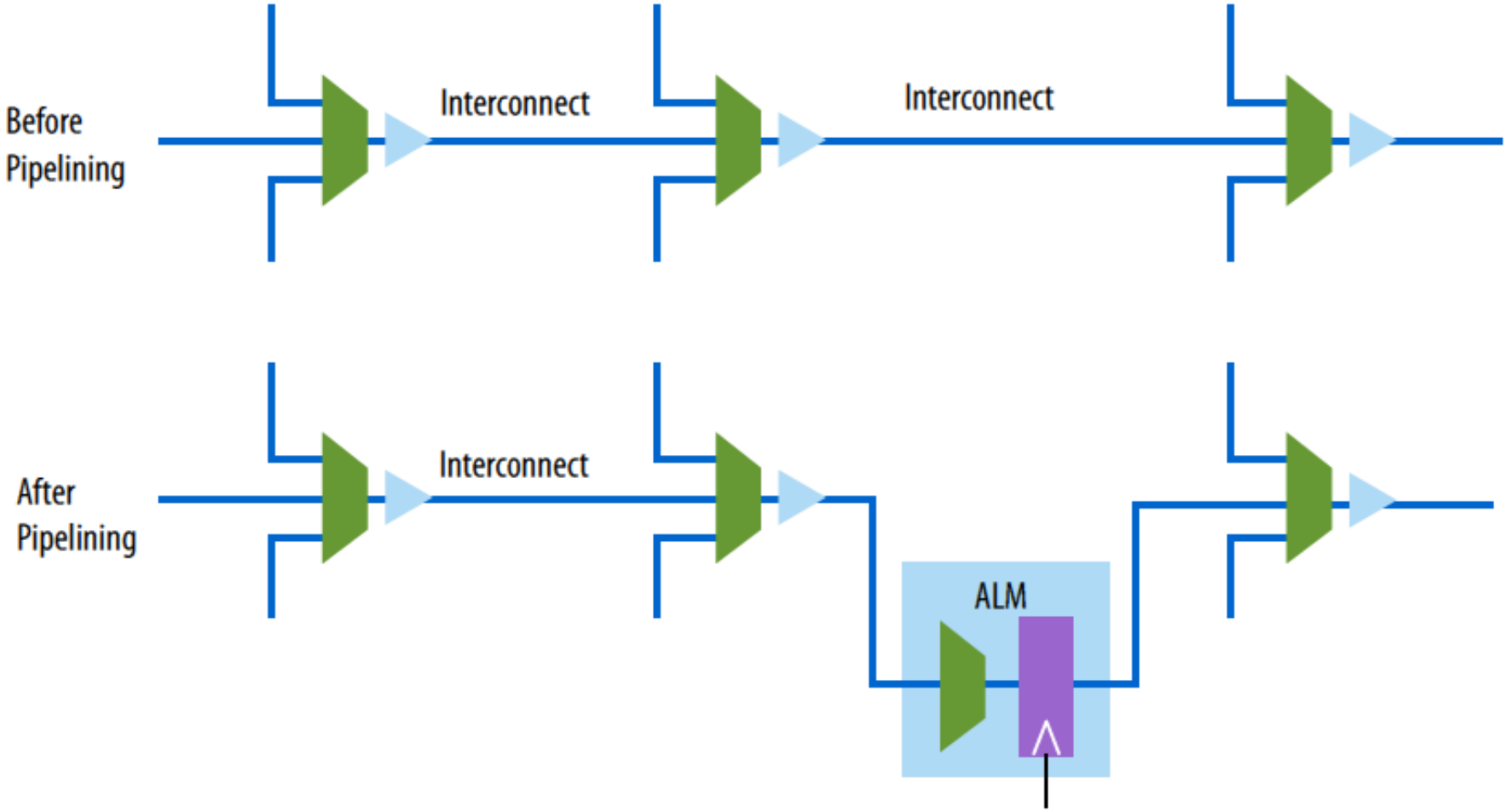
Stratix 10 Product Table

	Product Line	GX 500 SX 500	GX 650 SX 650	GX 850 SX 850	GX 1100 SX 1100	GX 1650 SX 1650	GX 2100 SX 2100	GX 2500 SX 2500	GX 2800 SX 2800	GX 4500 SX 4500	GX 5500 SX 5500
Resources	Logic elements (LEs)[1]	484,000	646,000	841,000	1,092,000	1,624,000	2,005,000	2,422,000	2,753,000	4,463,000	5,510,000
	Adaptive logic modules (ALMs)	164,160	218,880	284,960	370,080	550,540	679,680	821,150	933,120	1,512,820	1,867,680
	ALM registers	656,640	875,520	1,139,840	1,480,320	2,202,160	2,718,720	3,284,600	3,732,480	6,051,280	7,470,720
	Hyper-Registers from HyperFlex™ architecture	Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric									
	Programmable clock trees synthesizable	Hundreds of synthesizable clock trees									
	M20K memory blocks	2,196	2,583	3,477	4,401	5,851	6,501	9,963	11,721	7,033	7,033
	M20K memory size (Mb)	43	50	68	86	114	127	195	229	137	137
	MLAB memory size (Mb)	3	3	4	6	8	11	13	15	23	29
	Variable-precision digital signal processing (DSP) blocks	1,152	1,440	2,016	2,520	3,145	3,744	5,011	5,760	1,980	1,980
	18 x 19 multipliers	2,304	2,880	4,032	5,040	6,290	7,488	10,022	11,520	3,960	3,960
	Peak fixed-point performance (TMACS)[2]	4.6	5.8	8.1	10.1	12.6	15.0	20.0	23.0	7.9	7.9
	Peak floating-point performance (TFLOPS)[3]	1.8	2.3	3.2	4.0	5.0	6.0	8.0	9.2	3.2	3.2
I/O and Architectural Features	Secure device manager	AES-256/SHA-256 bitsream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side channel attack protection									
	Hard processor system[4]	Quad-core 64 bit ARM® Cortex®-A53 up to 1.5 GHz with 32 KB I/D cache, NEON™ coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general-purpose timers x7, watchdog timer x4									
	Maximum user I/O pins	488	488	736	736	704	704	1160	1160	1640	1640
	Maximum LVDS pairs 1.6 Gbps (RX or TX)	240	240	360	360	336	336	576	576	816	816
	Total full duplex transceiver count	24	24	48	48	96	96	144	144	72	72
	GXT full duplex transceiver count (up to 30 Gbps)	16	16	32	32	64	64	96	96	48	48
	GX full duplex transceiver count (up to 17.4 Gbps)	8	8	16	16	32	32	48	48	24	24
	PCI Express® (PCIe®) hard intellectual property (IP) blocks (Gen3 x16)	1	1	2	2	4	4	6	6	3	3
	Memory devices supported	DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys									
Package Options and I/O Pins: General-Purpose I/O (GPIO) Count, High-Voltage I/O Count, LVDS Pairs, and Transceiver Count[5, 6]											
F1152 pin (35 mm x 35 mm, 1.0 mm pitch)		344,8,168,24	344,8,168,24	–	–	–	–	–	–	–	–
F1760 pin (42.5 mm x 42.5 mm, 1.0 mm pitch)		488,8,240,24	488,8,240,24	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	688,16,336,48	–	–
F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)		–	–	736,16,360,48	736,16,360,48	–	–	–	–	–	–
F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)		–	–	–	–	648,24,312,72	648,24,312,72	648,24,312,72	648,24,312,72	–	–
F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)		–	–	–	–	464,32,216,96	464,32,216,96	–	–	–	–
F2112 pin (47.5 mm x 47.5 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	648,24,312,72	648,24,312,72
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)		–	–	–	–	–	–	1160,8,576,24	1160,8,576,24	1256,8,624,24	1256,8,624,24
F2397 pin (50 mm x 50 mm, 1.0 mm pitch)		–	–	–	–	704,32,336,96	704,32,336,96	704,32,336,96	704,32,336,96	–	–
F2597 pin (52.5 mm x 52.5 mm, 1.0 mm pitch)		–	–	–	–	–	–	432,48,216,144	432,48,216,144	–	–
F2912 pin (55 mm x 55 mm, 1.0 mm pitch)		–	–	–	–	–	–	–	–	1640,8,816,24	1640,8,816,24

Arquitectura de la serie Stratix 10




Stratix 10 HyperFlex
Routing Multiplexer
(with Hyper-Register)
Interconnect
CRAM
Config
clk
CRAM
Config


Before
Pipelining
Interconnect
Interconnect
After
Pipelining
Interconnect
ALM

Elemento lógico (Adaptive Logic Module, ALM)

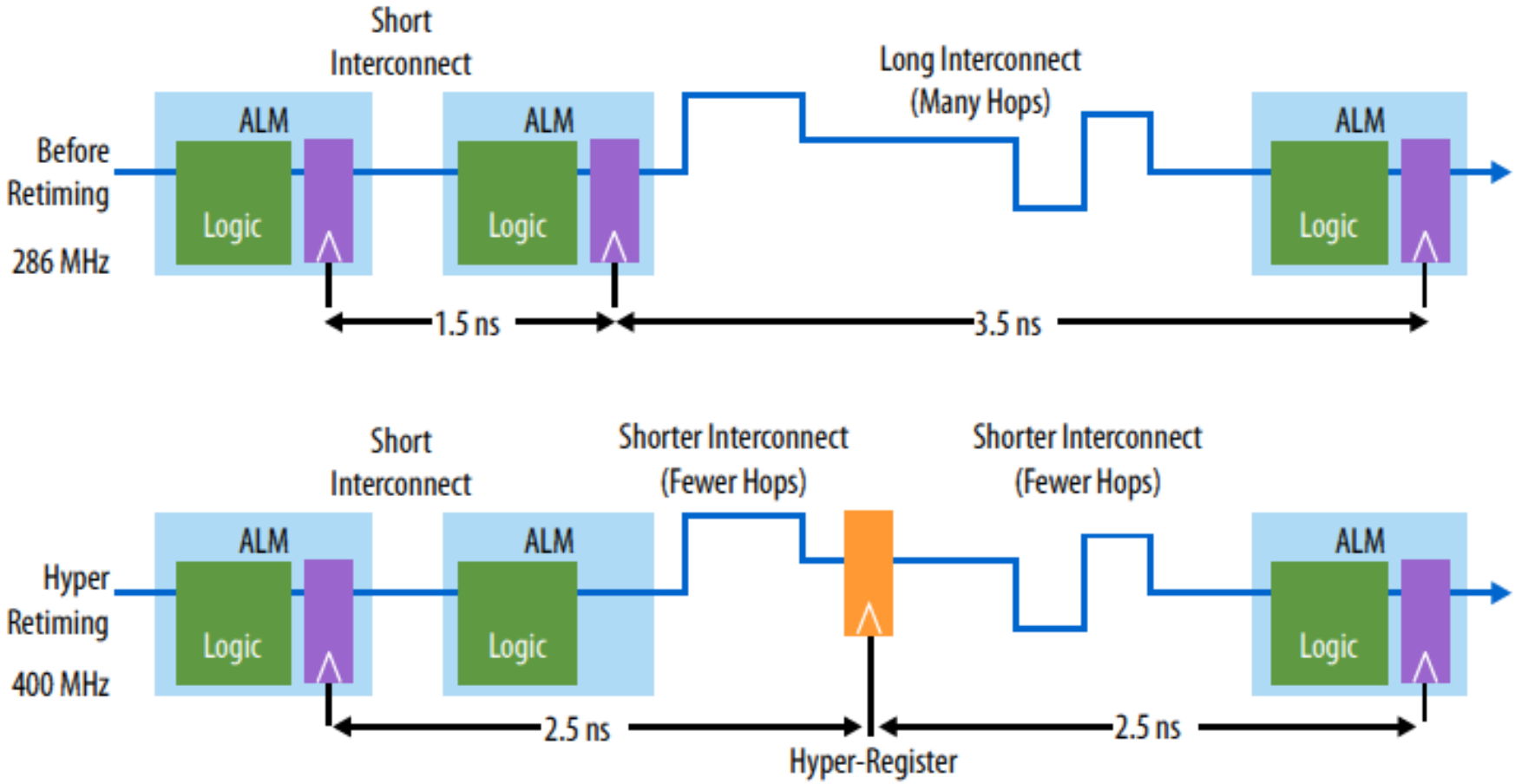


Figure 8. Placing Additional Pipeline Registers at the Input of a Clock Domain

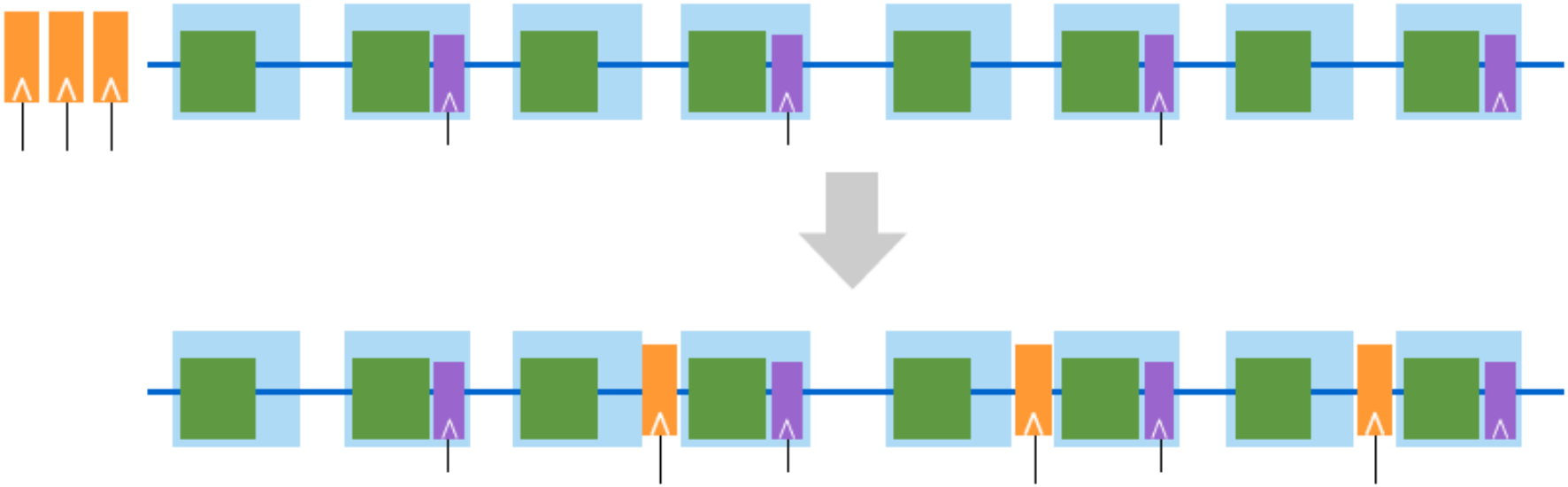


Figure 9. Hyper-Optimization of a Long Feedback Loop

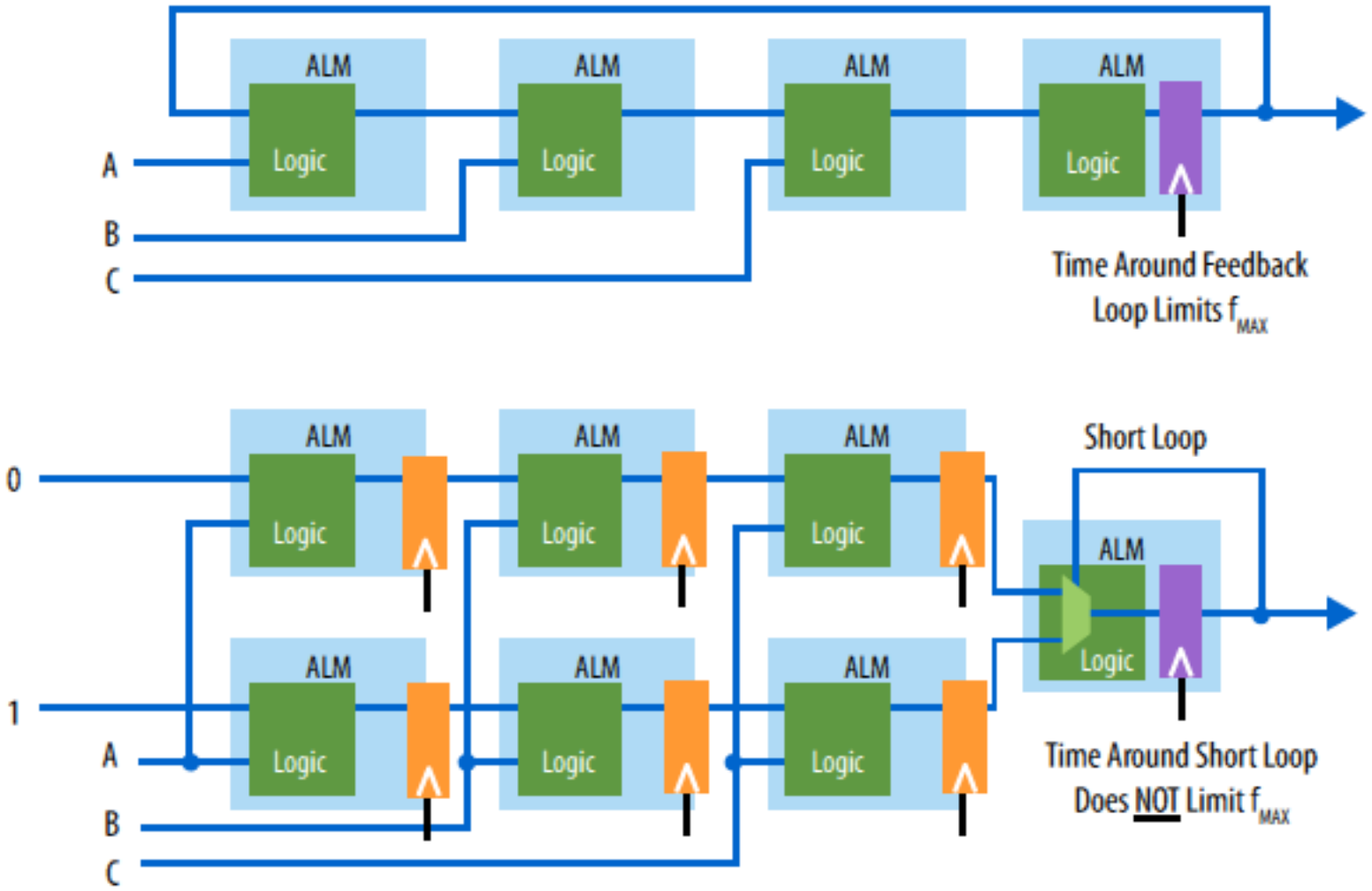
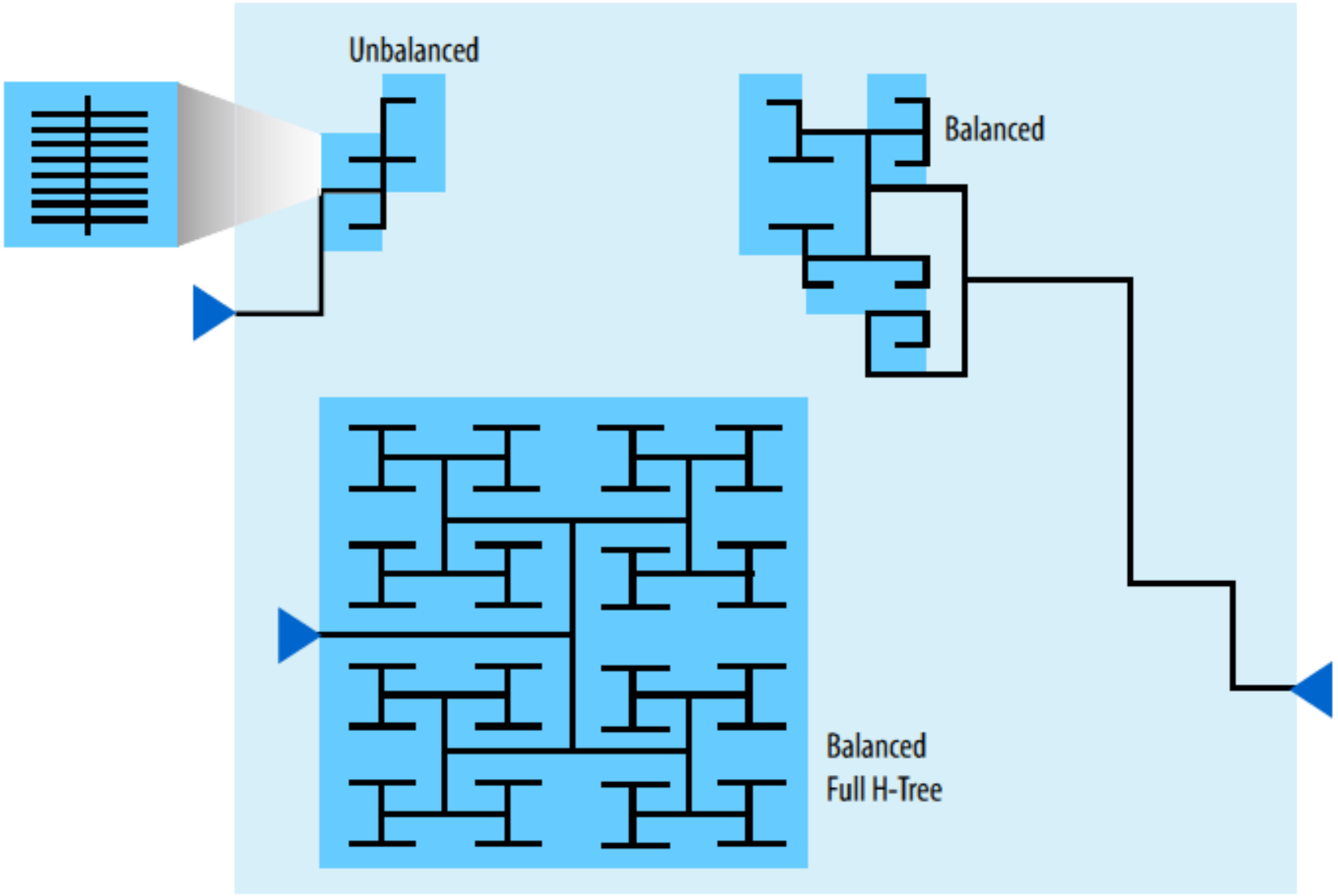


Figure 10. Balanced and Unbalanced Clock Tree Synthesis



Estándares Soportados

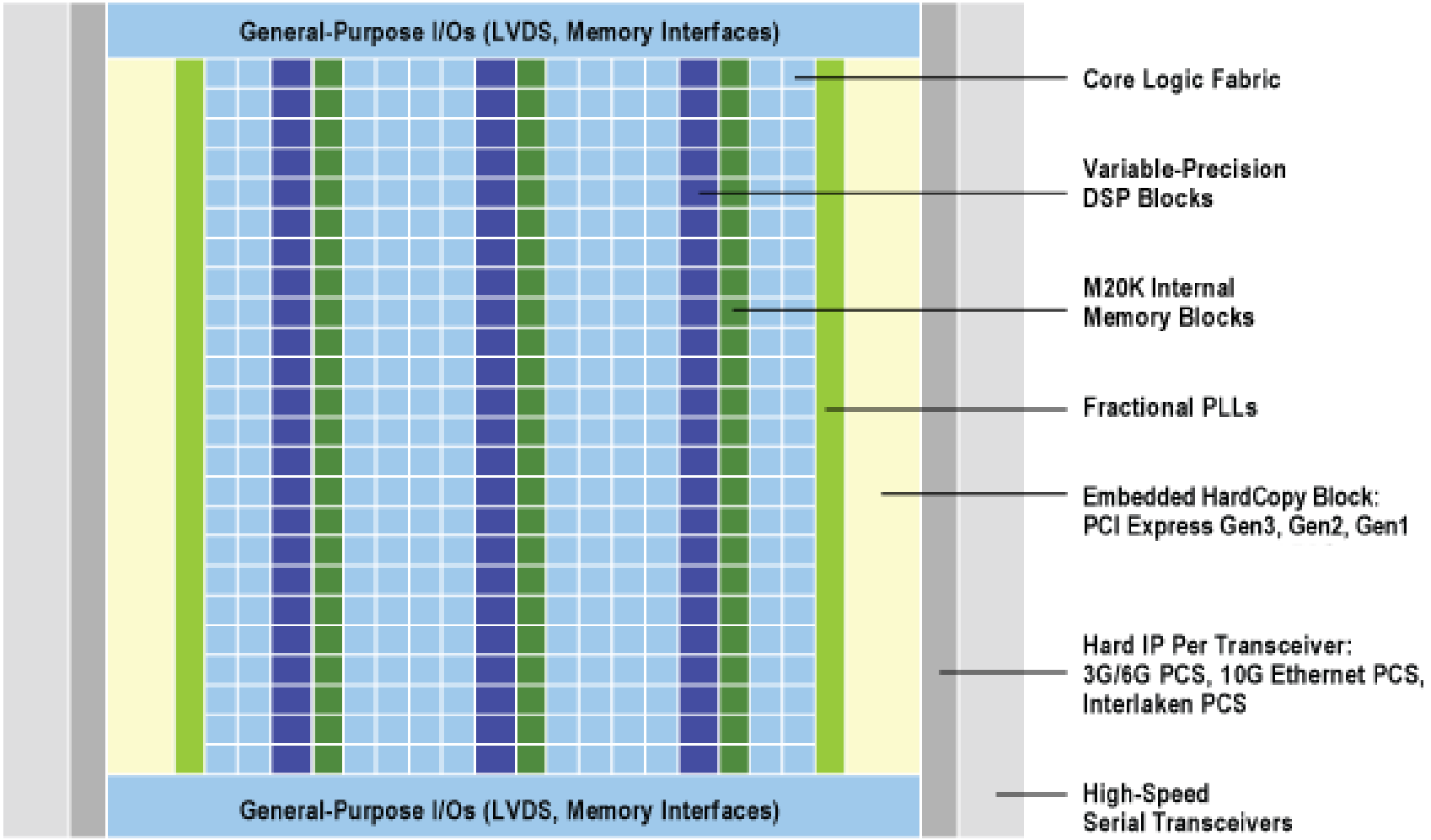
Table 7–1. Stratix III I/O Standard Applications (Part 1 of 2)

I/O Standard	Application
3.3-V LVTTL/LVCMOS	General purpose
3.0-V LVTTL/LVCMOS	General purpose
2.5-V LVTTL/LVCMOS	General purpose
1.8-V LVTTL/LVCMOS	General purpose
1.5-V LVTTL/LVCMOS	General purpose
1.2-V LVTTL/LVCMOS	General purpose
3.0-V PCI	PC and embedded system
3.0-V PCI-X	PC and embedded system
SSTL-2 Class I	DDR SDRAM
SSTL-2 Class II	DDR SDRAM
SSTL-18 Class I	DDR2 SDRAM
SSTL-18 Class II	DDR2 SDRAM
SSTL-15 Class I	DDR3 SDRAM
SSTL-15 Class II	DDR3 SDRAM
HSTL-18 Class I	QDRII/RLDRAM II
HSTL-18 Class II	QDRII/RLDRAM II
HSTL-15 Class I	QDRII/QDRII+/RLDRAM II
HSTL-15 Class II	QDRII/QDRII+/RLDRAM II
HSTL-12 Class I	General purpose
HSTL-12 Class II	General purpose
Differential SSTL-2 Class I	DDR SDRAM
Differential SSTL-2 Class II	DDR SDRAM
Differential SSTL-18 Class I	DDR2 SDRAM
Differential SSTL-18 Class II	DDR2 SDRAM
Differential SSTL-15 Class I	DDR3 SDRAM
Differential SSTL-15 Class II	DDR3 SDRAM
Differential HSTL-18 Class I	Clock interfaces
Differential HSTL-18 Class II	Clock interfaces
Differential HSTL-15 Class I	Clock interfaces
Differential HSTL-15 Class II	Clock interfaces
Differential HSTL-12 Class I	Clock interfaces
Differential HSTL-12 Class II	Clock interfaces

Table 7–1. Stratix III I/O Standard Applications (Part 2 of 2)

I/O Standard	Application
LVDS	High-speed communications
RSDS	Flat panel display
mini-LVDS	Flat panel display
LVPECL	Video graphics and clock distribution

Feature	Stratix V E FPGA	Stratix V GS FPGA	Stratix V GX FPGA	Stratix V GT FPGA
High-performance adaptive logic modules (ALMs)	359,200	262,400	359,200	234,720
Variable-precision DSP blocks (18x18)	704	3,926	798	512
M20K memory blocks	2,640	2,567	2,660	2,560
External memory interface	OK	OK	OK	OK
Partial reconfiguration	OK	OK	OK	OK
fPLL	OK	OK	OK	OK
Design security	OK	OK	OK	OK
SEU mitigation	OK	OK	OK	OK
PCI Express Gen3, Gen2, Gen1 hard IP blocks	-	Up to 2	Up to 4	1
Embedded HardCopy Blocks	-			


General-Purpose I/Os (LVDS, Memory Interfaces)
Core Logic Fabric
Variable-Precision
DSP Blocks
M20K Internal
Memory Blocks
Fractional PLLs
Embedded HardCopy Block:
PCI Express Gen3, Gen2, Gen1
Hard IP Per Transceiver:
3G/6G PCS, 10G Ethernet PCS,
Interlaken PCS
High-Speed
Serial Transceivers
General-Purpose I/Os (LVDS, Memory Interfaces)

Stratix V FPGA Applications

Stratix V FPGAs address the design challenges for applications in a variety of industries. Expand the sections below for details about specific applications.

- 100-Gb Optical Transport Network (OTN) Multiplexing Transponder
- 100 Gigabit Ethernet (GbE) Line Card
- Crossbar and Backplane Switch Fabric
- Military Radar Application
- RF Card and Channel Card
- Studio Video Server

Microsemi (antigua ACTEL)

Mecanismo de programación basado en antifusibles:

- ☺ Altas prestaciones
- ☹ Programable una sola vez

Organización de las células lógicas en estilo Gate-Array, con los canales de interconexión entre las filas.

Capacidad típica: 35K puertas

Posee familias con tolerancia a la radiación cósmica, útil en aplicaciones espaciales (54SX).

Tecnologías de 0,45mm y 3 niveles de metal, especiales

Equipos de desarrollo específicos para estos dispositivos.

Típicamente alcanzan 60MHz y son compatibles PCI???

Los diseños están protegidos por la propia configuración del sistema

Familia de Productos Microsemi

Categoría	Nombre	Tecnología	Capacidad
Flash FPGA	ProASIC3	Flash	3M
FPGA	IGLOO	Flash, Low power	3M
FPGA	Axcelerator	Antifusible	2M
Espacial	RTSX / RTAX	Antifusible	108K
Militar / Aeroespacial	ProASIC Plus	Antifusible	108K
Mixta	Fusion		

SmartFusion Devices

SmartFusion Devices		A2F060	A2F200	A2F500
FPGA Fabric	System Gates	60,000	200,000	500,000
	Tiles (D-flip-flops)	1,536	4,606	11,520
	RAM Blocks (4,606 bits)	8	8	24
Microcontroller Subsystem (MSS)	Flash (Kbytes)	128	256	512
	SRAM (Kbytes)	16	64	64
	Cortex-M3 with Memory Protection Unit (MPU)	Yes	Yes	Yes
	10/100 Ethernet MAC	No	Yes	Yes
	External Memory Controller (EMC)	24-bit address, 16-bit data	24-bit address, 16-bit data	24-bit address, 16-bit data[1]
	DMA	8 Ch	8 Ch	8 Ch
	I^2C	2	2	2
	SPI	2	2	2
	16550 UART	2	2	2
	32-Bit Timer	2	2	2
	PLL	1	1	2[2]
	32 KHz Low Power Oscillator	1	1	1
	100 MHz On-Chip RC Oscillator	1	1	1
	Main Oscillator (32 KHz to 20 MHz)	1	1	1
Programmable Analog	ADCs (8-/10-/12-bit SAR)	1	2	3[4]
	DACs (12-bit sigma-delta)	1	2	3[4]
	Signal Conditioning Blocks (SCBs)	1	4	5[4]
	Comparators[3]	2	8	10[4]
	Current Monitors[3]	1	4	5[4]
	Temperature Monitors[3]	1	4	5[4]
	Bipolar High Voltage Monitors[3]	2	8	10[4]

IGLOO/e Devices

IGLOO Devices	AGL030	AGL060	AGL125	AGL250	AGL400	AGL600	AGL1000	AGLE600	AGLE3000
Cortex-M1 Devices[1]				M1AGL250		M1AGL600	M1AGL1000		M1AGLE3000
System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	3,000,000
Typical Equivalent Macrocells	256	512	1,024	2,048	–	–	–	–	–
VersaTiles (D-flip-flops)	768	1,536	3,072	6,144	9,216	13,824	24,576	13,824	75,264
Flash*Freeze Mode (typical, µW)	5	10	16	24	32	36	53	49	137
RAM (1,024 bits)	–	18	36	36	54	108	144	108	504
RAM Blocks (4,608 bits)	–	4	8	8	12	24	32	24	112
FlashROM Kbits (1,024 bits)	1	1	1	1	1	1	1	1	1
AES-Protected ISP[1]	–	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLLs with CCC[2]	–	1	1	1	1	1	1	6	6
VersaNet Globals[3]	6	18	18	18	18	18	18	18	18
I/O Banks	2	2	2	4	4	4	4	8	8
Maximum User I/Os (packaged device)	81	96	133	143	194	235	300	270	620
Package Pins									
UC	UC81								
CS	CS81	CS121	CS81 CS196	CS81 CS196[4]	CS196	CS281	CS281		
QN	QN48 QN68 QN132	QN132	QN132	QN132[4]					
VQ	VQ100	VQ100	VQ100	VQ100					
FG		FG144[5]	FG144	FG144	FG144 FG256 FG484	FG144 FG256 FG484	FG144 FG256 FG484	FG256 FG484	FG484 FG896

Notes:

ProASIC3/E Devices

ProASIC3/E Devices	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000	A3PE600	A3PE1500	A3PE3000
Cortex-M1 Devices				M1A3P250	M1A3P400	M1A3P600	M1A3P1000		M1A3PE1500	M1A3PE3000
System Gates	30,000	60,000	125,000	250,000	400,000	600,000	1,000,000	600,000	1,500,000	3,000,000
Typical Equivalent Macrocells	256	512	1,024	2,048	–	–	–	–	–	–
VersaTiles (D-flip-flops)	768	1,536	3,072	6,144	9,216	13,824	24,576	13,824	38,400	75,264
RAM (1,024 bits)	–	18	36	36	54	108	144	108	270	504
4,608-Bit Blocks	–	4	8	8	12	24	32	24	60	112
FlashROM Kbits (1,024 bits)	1	1	1	1	1	1	1	1	1	1
AES-Protected ISP[1]	–	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	–	1	1	1	1	1	1	6	6	6
VersaNet Globals	6	18	18	18	18	18	18	18	18	18
I/O Banks	2	2	2	4	4	4	4	8	8	8
Maximum User I/Os (packaged device)	81	96	133	157	194	235	300	270	444	620
Package Pins										
QFN	QN48 QN68 QN132	QN132	QN132[2]	QN132[2, 3]						
CS		CS121								
VQ	VQ100	VQ100[2]	VQ100[2]	VQ100[2]						
TQ		TQ144	TQ144							
PQ			PQ208	PQ208	PQ208	PQ208	PQ208	PQ208	PQ208	PQ208
FG		FG144[2]	FG144[2]	FG144[2] FG256[2, 3]	FG144 FG256 FG484	FG144 FG256 FG484	FG144[2] FG256[2] FG484[2]	FG256 FG484	FG484 FG676	FG324 FG484 FG896

Table 1 • RTAX Family Product Profile

Device	RTAX250S/SL	RTAX1000S/SL	RTAX2000S/SL	RTAX4000S/SL	RTAX2000D/DL	RTAX4000D/DL
Capacity						
Equivalent System Gates	250,000	1,000,000	2,000,000	4,000,000	2,000,000	4,000,000
ASIC Gates	30,000	125,000	250,000	500,000	250,000	500,000
Modules						
Register (R-cells)	1,408	6,048	10,752	20,160	9,856	18,480
Combinatorial (C-cells)	2,816	12,096	21,504	40,320	19,712	36,960
Embedded RAM/FIFO (w/o EDAC)						
Core RAM Blocks	12	36	64	120	64	120
Core RAM Bits (K = 1,024)	54 k	162 k	288 k	540 k	288 k	540 k
Embedded Multiply/Accumulate Blocks	–	–	–	–	64	120
Clocks (segmentable)						
Hardwired	4	4	4	4	4	4
Routed	4	4	4	4	4	4
I/Os						
I/O Banks	8	8	8	8	8	8
User I/Os (maximum)	198	418	684	840	684	840
I/O Registers	744	1,548	2,052	2,520	2,052	2,520
Package						
CCGA/LGA*	624	624	624, 1152	1272	1272	1272
CQFP	208, 352	352	256, 352	352	352	352

Note: **The body size of the 1272-pin CCGA and LGA packages used on the RTAX-DSP devices is slightly larger than the body size of the 1272-pin CCGA and LGA used on the RTAX4000S/SL devices.*

Infrastructura

ProASIC Plus

Features and Benefits

High Capacity

Commercial and Industrial

- 75,000 to 1 Million System Gates
- 27 k to 198 kbits of Two-Port SRAM
- 66 to 712 User I/Os

Military

- 300, 000 to 1 million System Gates
- 72 k to 198 kbits of Two Port SRAM
- 158 to 712 User I/Os

Reprogrammable Flash Technology

- 0.22 µm 4 LM Flash-Based CMOS Process
- Live At Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- No Configuration Device Required
- Retains Programmed Design during Power-Down/Up Cycles
- Mil/Aero Devices Operate over Full Military Temperature Range

Performance

- 3.3 V, 32-Bit PCI, up to 50 MHz (33 MHz over military temperature)
- Two Integrated PLLs
- External System Performance up to 150 MHz

Secure Programming

- The Industry's Most Effective Security Key (FlashLock®)

Low Power

- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small, Efficient, Configurable (Combinatorial or Sequential) Logic Cells

High Performance Routing Hierarchy

- Ultra-Fast Local and Long-Line Network
- High-Speed Very Long-Line Network
- High-Performance, Low Skew, Splittable Global Network
- 100% Routability and Utilization

I/O

- Schmitt-Trigger Option on Every Input
- 2.5 V/3.3 V Support with Individually-Selectable Voltage and Slew Rate
- Bidirectional Global I/Os
- Compliance with PCI Specification Revision 2.2
- Boundary-Scan Test IEEE Std. 1149.1 (JTAG) Compliant
- Pin Compatible Packages across the ProASIC^{PLUS} Family

Unique Clock Conditioning Circuitry

- PLL with Flexible Phase, Multiply/Divide and Delay Capabilities
- Internal and/or External Dynamic PLL Configuration
- Two LVPECL Differential Pairs for Clock or Data Inputs

Standard FPGA and ASIC Design Flow

- Flexibility with Choice of Industry-Standard Front-End Tools
- Efficient Design through Front-End Timing and Gate Optimization

ISP Support

- In-System Programming (ISP) via JTAG Port

SRAMs and FIFOs

- SmartGen Netlist Generation Ensures Optimal Usage of Embedded Memory Blocks
- 24 SRAM and FIFO Configurations with Synchronous and Asynchronous Operation up to 150 MHz (typical)

Arquitectura ProASIC Plus

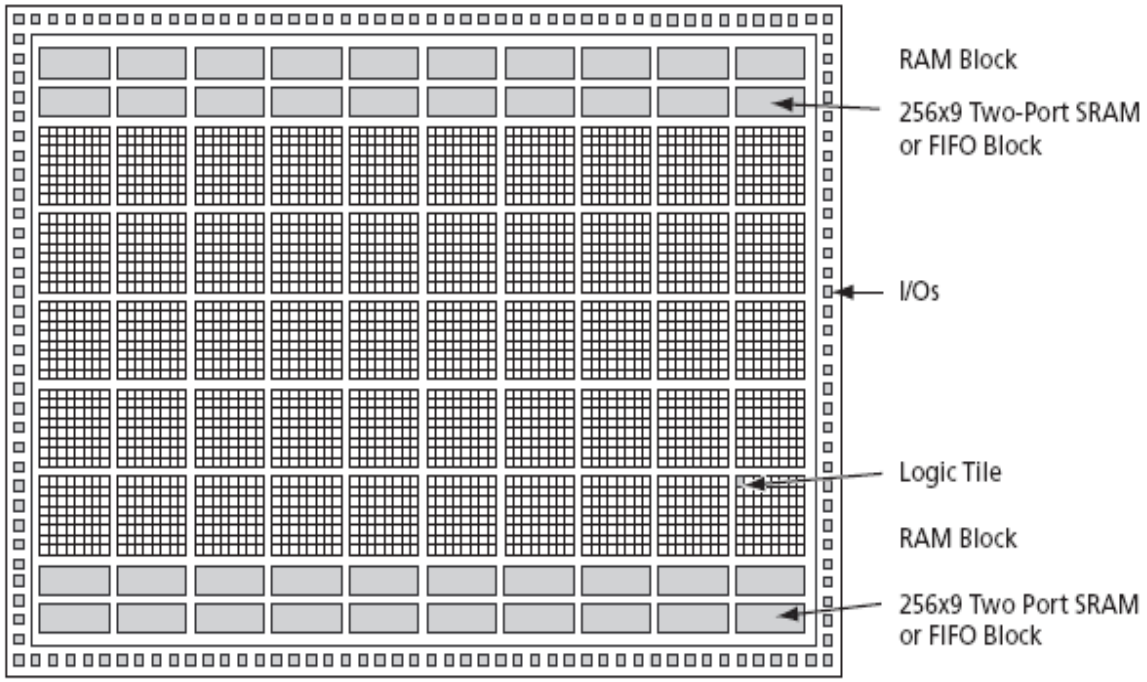
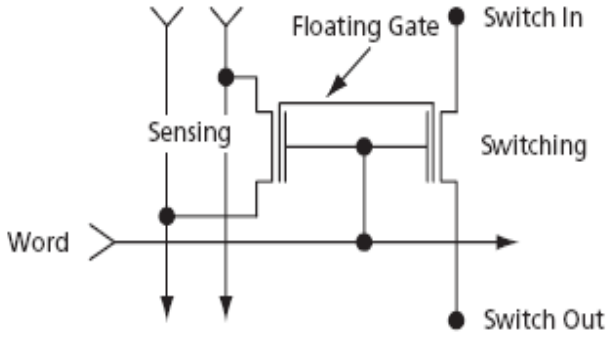
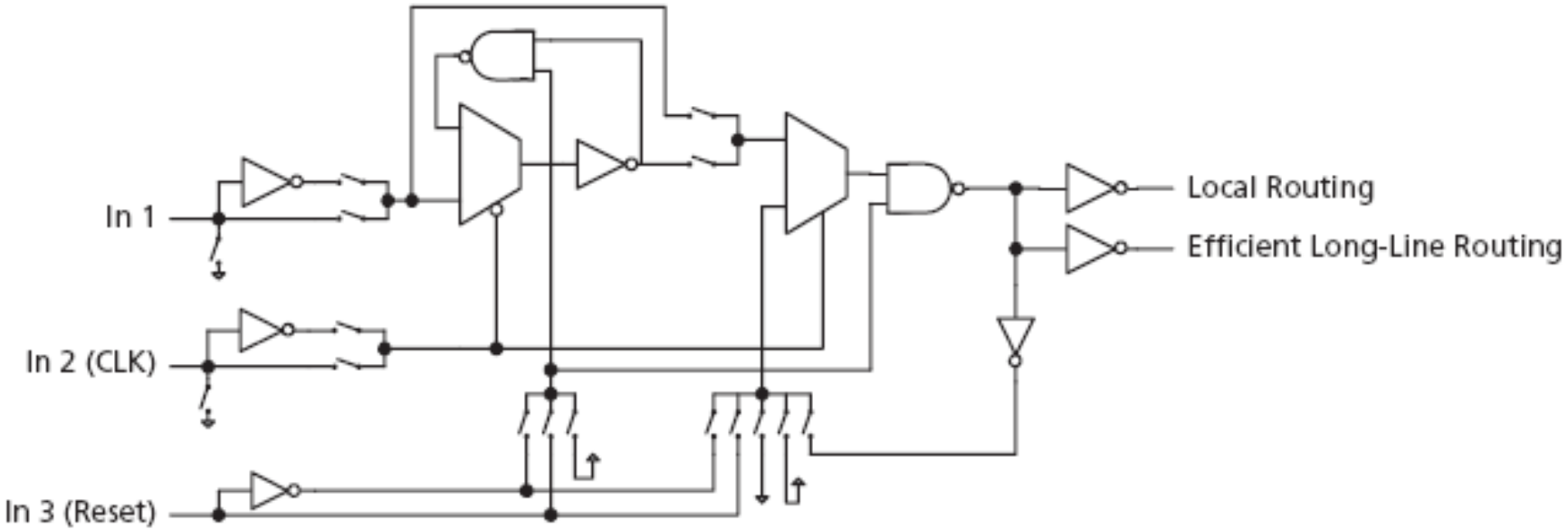


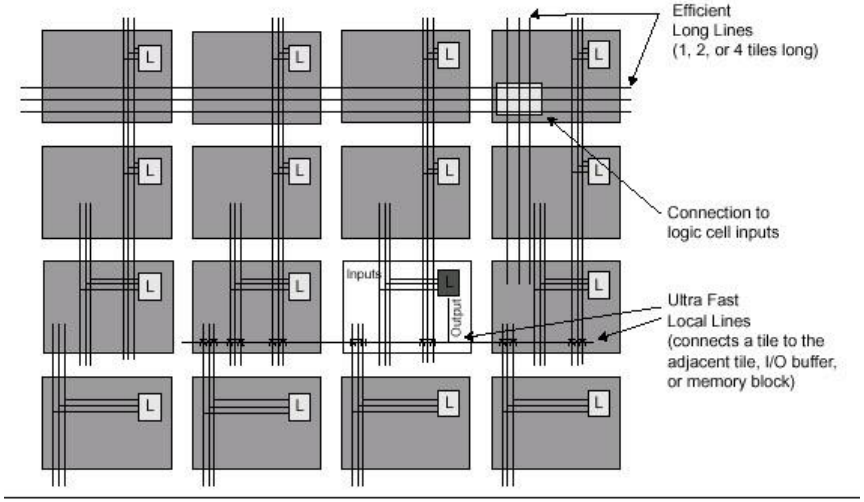
Figure 1-1 • **The ProASIC^{PLUS} Device Architecture**

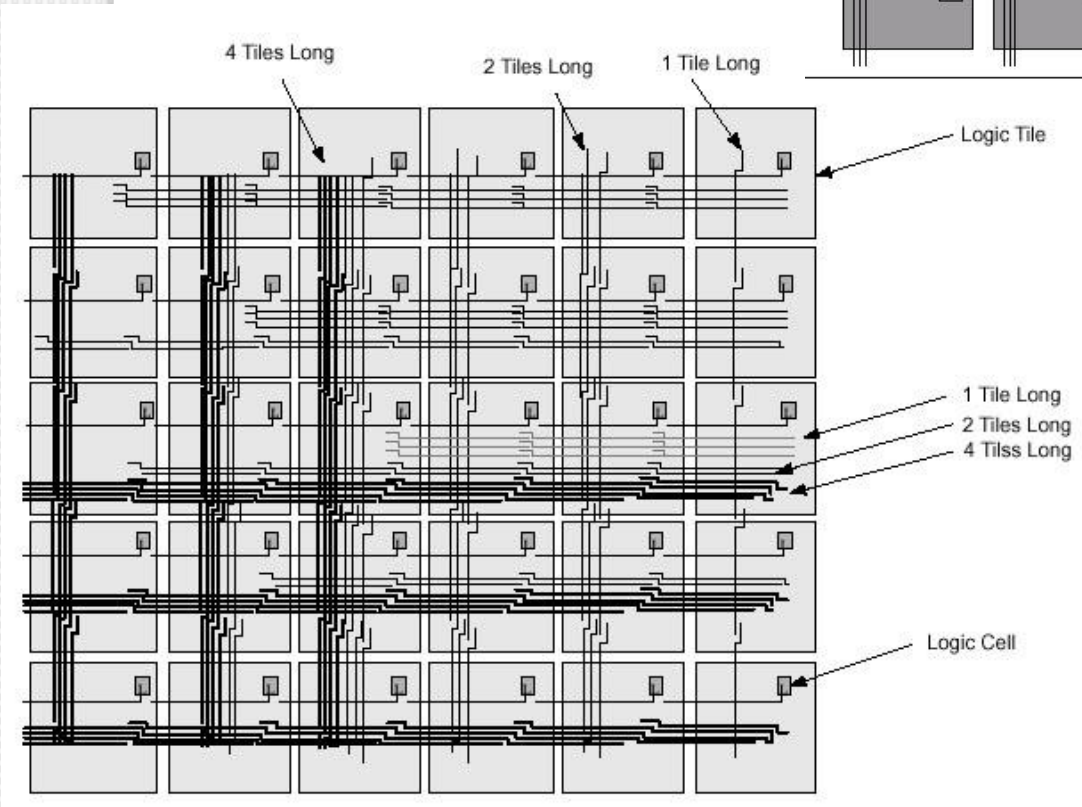


Célula Básica



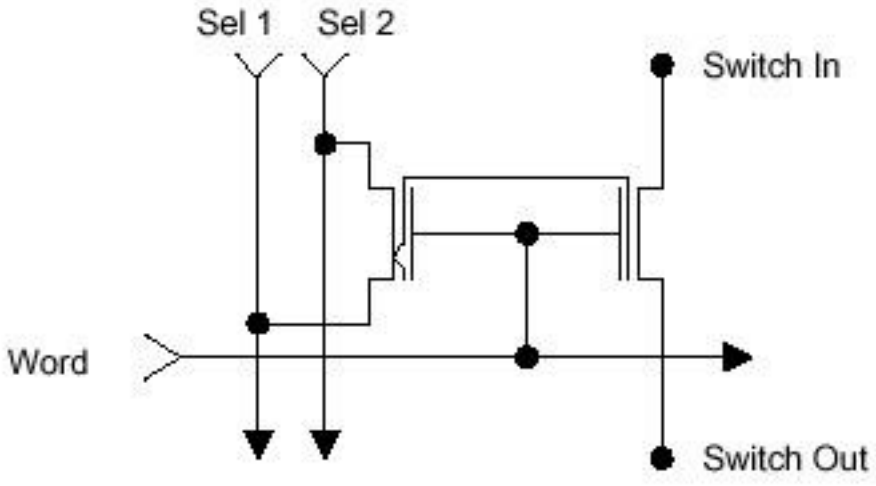
Recursos de Rutado



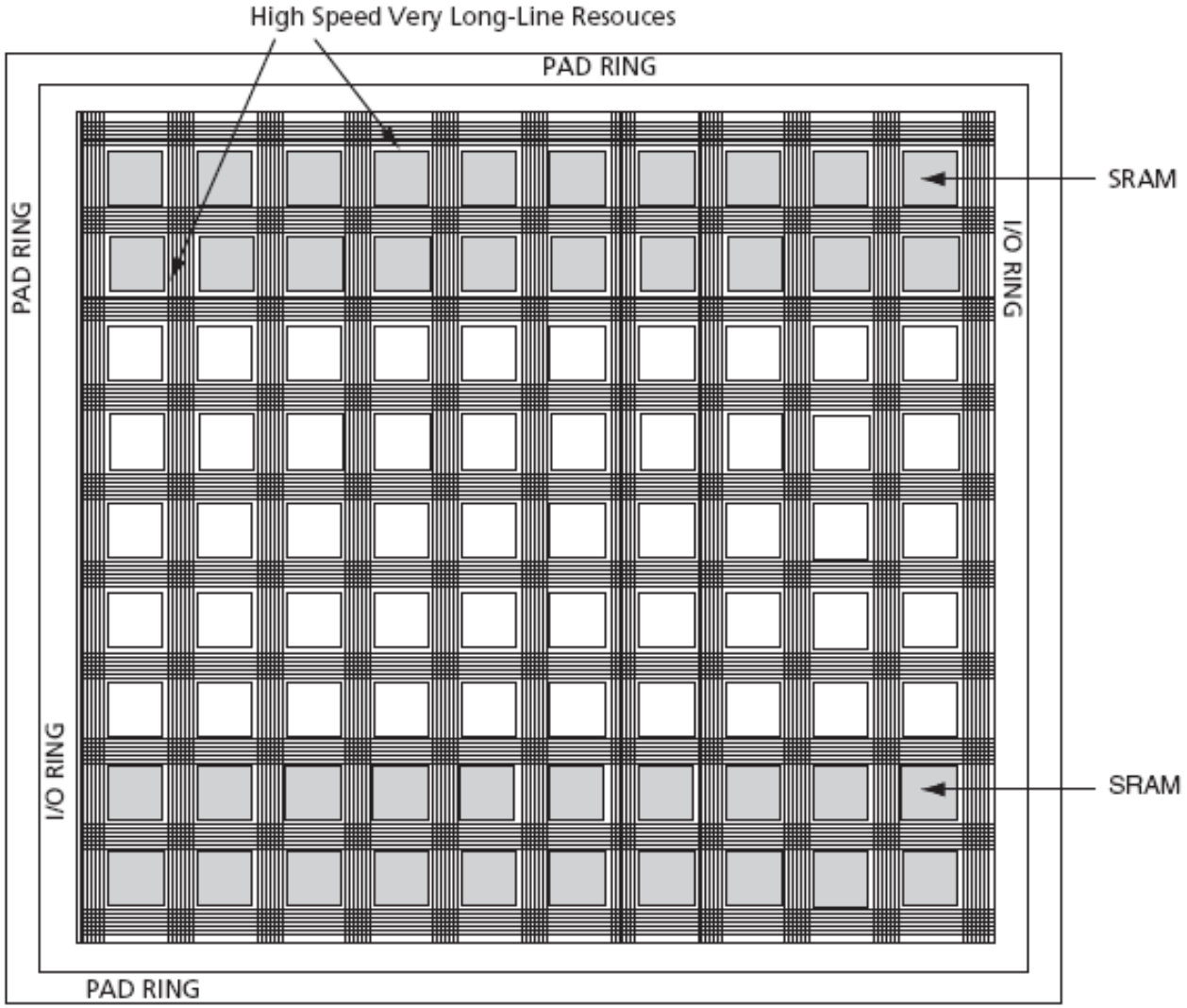


Mecanismo de Programación

Control del *switch* de programación mediante un segundo transistor que transfiere la carga a la puerta flotante. Mediante la activación de las tensiones en sel1 y sel2 se inyecta o se extrae la carga y mediante la línea word el punto de programación es seleccionado

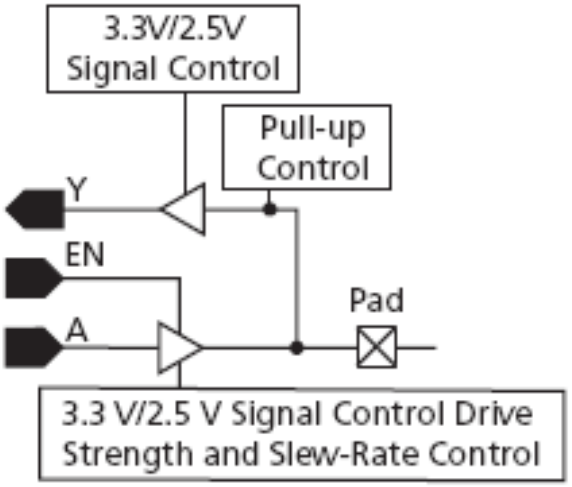


Arquitectura Global

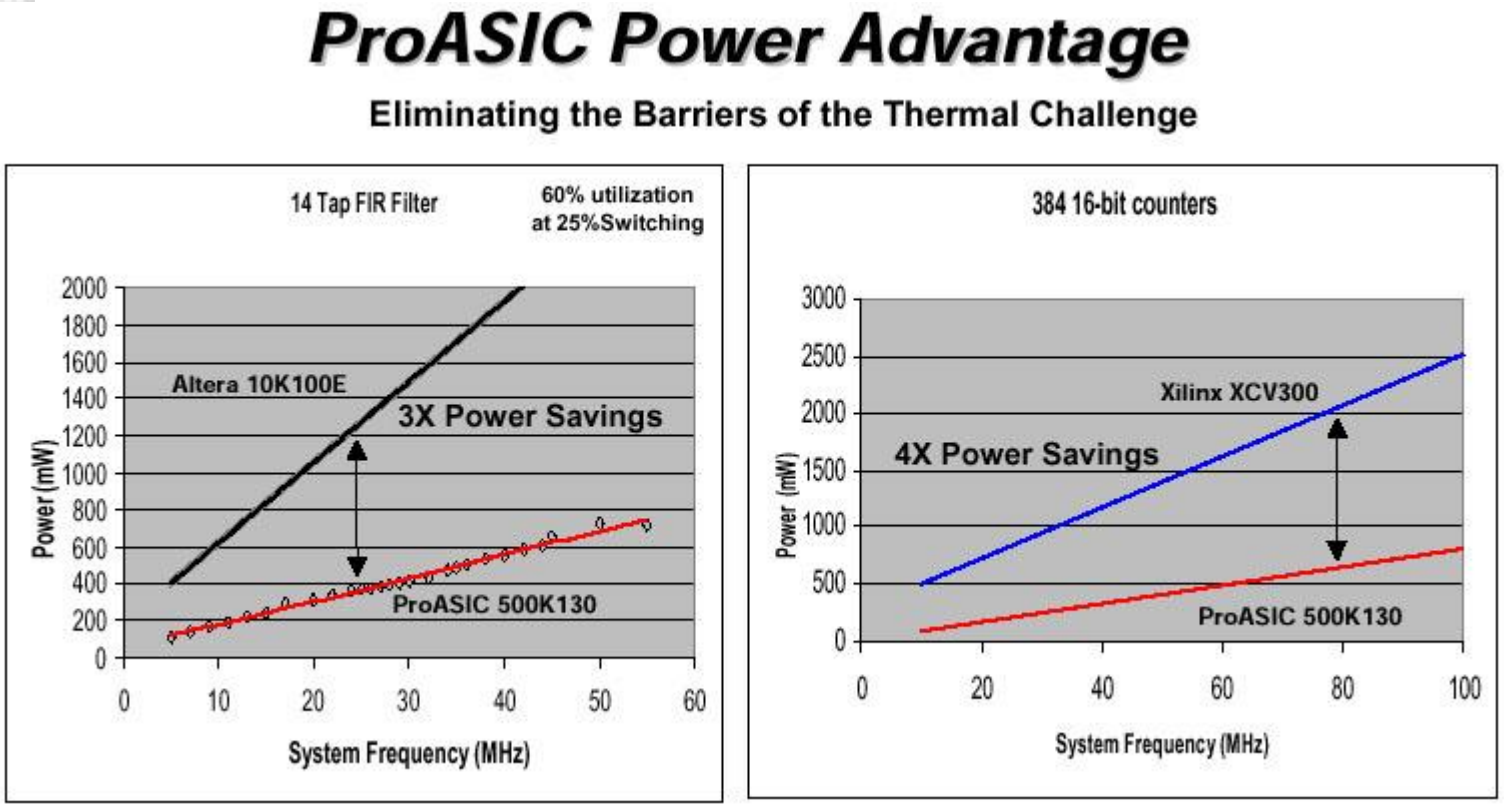


Interconexiones I/Os

Function	Description
I/O pads configured as inputs	• Selectable 2.5 V or 3.3 V threshold levels • Optional pull-up resistor • Optionally configurable as Schmitt trigger input. The Schmitt trigger input option can be configured as an input only, not a bidirectional buffer. This input type may be slower than a standard input under certain conditions and has a typical hysteresis of 0.35 V. I/O macros with an "S" in the standard I/O library have added Schmitt capabilities. • 3.3 V PCI Compliant (except Schmitt trigger inputs)
I/O pads configured as outputs	• Selectable 2.5 V or 3.3 V compliant output signals • 2.5 V – JEDEC JESD 8-5 • 3.3 V – JEDEC JESD 8-A (LVTTL and LVCMOS) • 3.3 V PCI compliant • Ability to drive LVTTL and LVCMOS levels • Selectable drive strengths • Selectable slew rates • Tristate
I/O pads configured as bidirectional buffers	• Selectable 2.5 V or 3.3 V compliant output signals • 2.5 V – JEDEC JESD 8-5 • 3.3 V – JEDEC JESD 8-A (LVTTL and LVCMOS) • 3.3 V PCI compliant • Optional pull-up resistor • Selectable drive strengths • Selectable slew rates • Tristate



Consumo de potencia



FPGA Fusion

Fusion Family of Mixed-Signal Flash FPGAs with Optional Soft ARM® Support

FlashLock®

Features and Benefits

High-Performance Reprogrammable Flash Technology
- Advanced 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Nonvolatile, Retains Program when Powered Off
- Live at Power-Up (LAPU) Single-Chip Solution
- 350 MHz System Performance

Embedded Flash Memory
- User Flash Memory – 2 Mbits to 8 Mbits
  - Configurable 8-, 16-, or 32-Bit Datapath
  - 10 ns Access in Read-Ahead Mode
- 1 kbit of Additional FlashROM

Integrated A/D Converter (ADC) and Analog I/O
- Up to 12-Bit Resolution and up to 600 ksps
- Internal 2.56 V or External Reference Voltage
- ADC: Up to 30 Scalable Analog Input Channels
- High-Voltage Input Tolerance: –10.5 V to +12 V
- Current Monitor and Temperature Monitor Blocks
- Up to 10 MOSFET Gate Driver Outputs
  - P- and N-Channel Power MOSFET Support
  - Programmable 1, 3, 10, 30 µA and 20 mA Drive Strengths
- ADC Accuracy is Better than 1%

On-Chip Clocking Support
- Internal 100 MHz RC Oscillator (accurate to 1%)
- Crystal Oscillator Support (32 kHz to 20 MHz)
- Programmable Real-Time Counter (RTC)
- 6 Clock Conditioning Circuits (CCCs) with 1 or 2 Integrated PLLs
  - Phase Shift, Multiply/Divide, and Delay Capabilities
  - Frequency: Input 1.5–350 MHz, Output 0.75–350 MHz

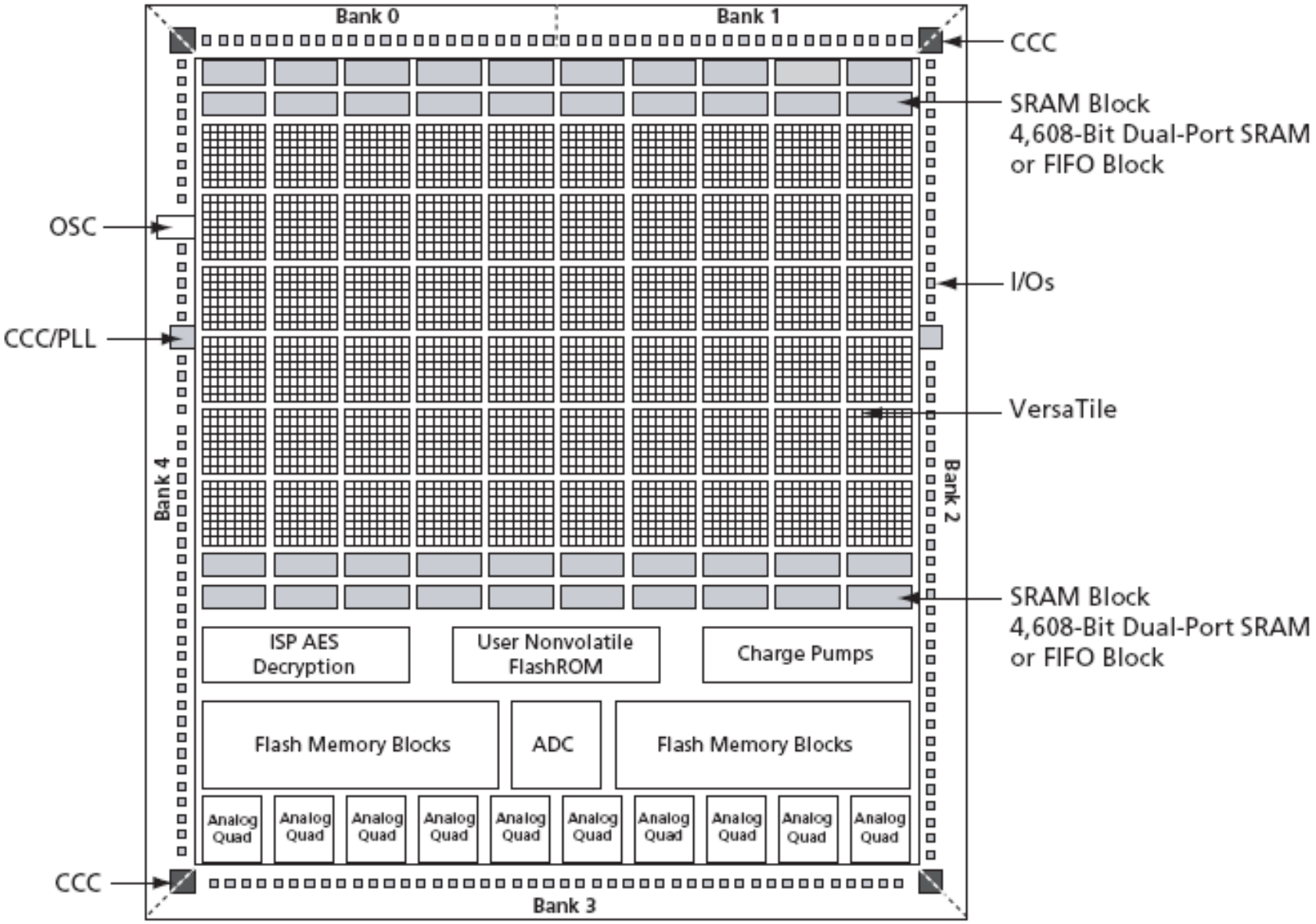
Low Power Consumption
- Single 3.3 V Power Supply with On-Chip 1.5 V Regulator
- Sleep and Standby Low Power Modes

In-System Programming (ISP) and Security
- Secure ISP with 128-Bit AES via JTAG
- FlashLock® to Secure FPGA Contents

Advanced Digital I/O
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages – Up to 5 Banks per Chip
- Single-Ended I/O Standards: LVTTL, LVCMOS 3.3 V / 2.5 V /1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, BLVDS, and M-LVDS
  - Built-In I/O Registers
  - 700 Mbps DDR Operation
- Hot-Swappable I/Os
- Programmable Output Slew Rate, Drive Strength, and Weak Pull-Up/Down Resistor
- Pin-Compatible Packages across the Fusion Family

SRAMs and FIFOs
- Variable-Aspect-Ratio 4,608-Bit SRAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)
- True Dual-Port SRAM (except ×18)
- Programmable Embedded FIFO Control Logic

Soft ARM7™ Core Support in M7 and M1 Fusion Devices
- CortexM1 (without debug), CoreMP7Sd (with debug) and CoreMP7S (without debug)


Bank 0
Bank 1
Bank 2
Bank 3
Bank 4
CCC
SRAM Block
4,608-Bit Dual-Port SRAM
or FIFO Block
I/Os
VersaTile
SRAM Block
4,608-Bit Dual-Port SRAM
or FIFO Block
OSC
CCC/PLL
CCC
ISP AES
Decryption
User Nonvolatile
FlashROM
Charge Pumps
Flash Memory Blocks
ADC
Flash Memory Blocks
Analog
Quad

Apéndice: FPGAs para aplicaciones aeroespaciales. Propuesta de Microsemi

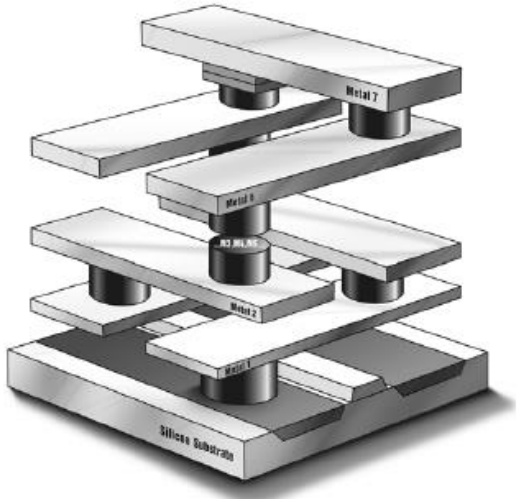
Rad Hard: RTAX

Rad Tol: RTSX

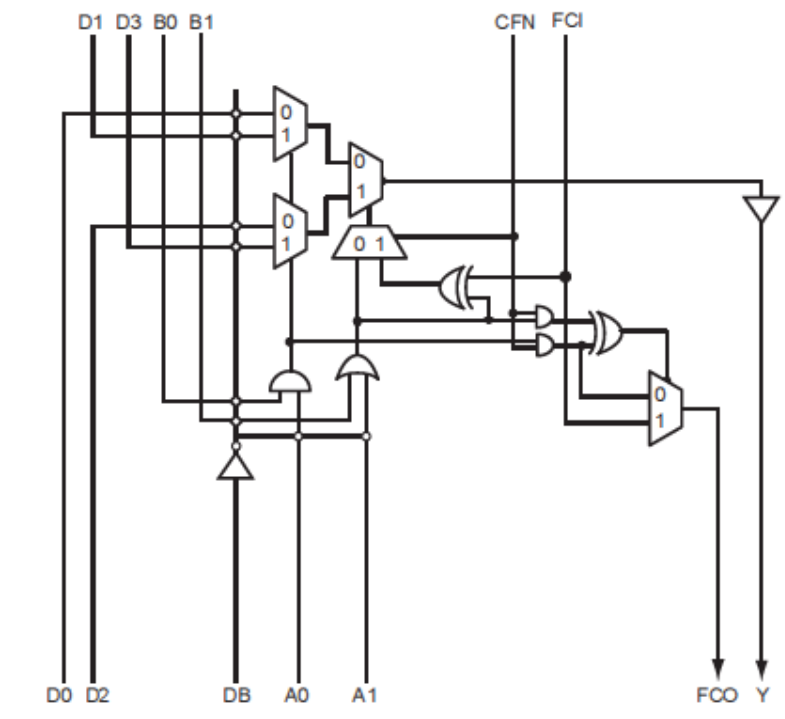
Military/Aerospace: ProASIC^{PLUS}

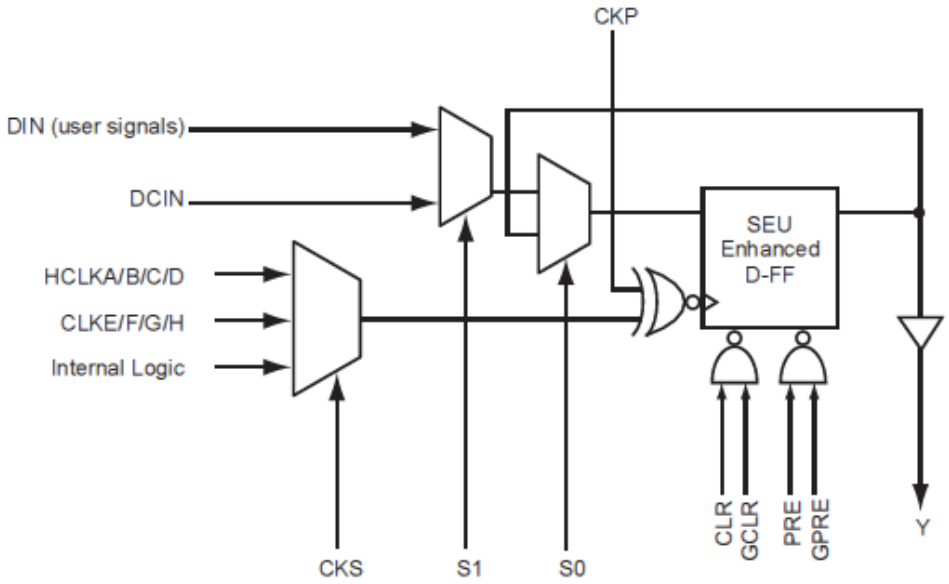
RTAX

- Equivalentes a las Axelerator
- RATX-S/SL y RATX-DSP
- Proceso de UMC de 150nm.Antifusible



Bloques Básicos funcionales C y R





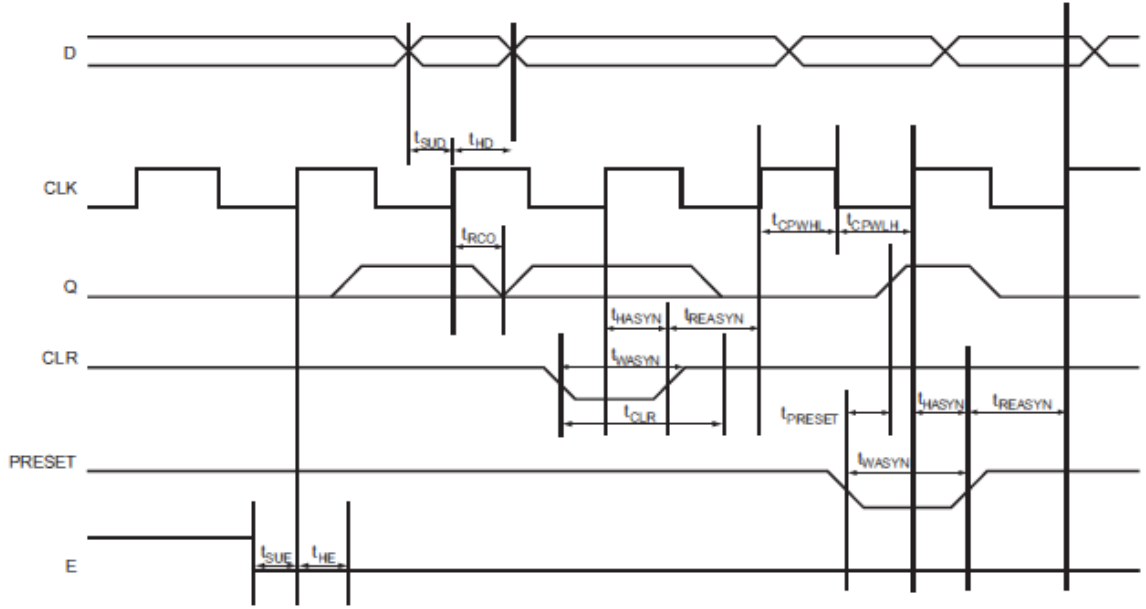


Figure 2-36 • R-Cell Delays

Timing Characteristics

Table 2-64 • Worst-Case Military Conditions VCCA = 1.425 V, VCCI = 3.0 V, T_J = 125°C

Parameter	Description	–1 Speed				Std. Speed		Units
		RTAX4000S/SL		RTAX250/1000/2000S/SL		All		
		Min.	Max.	Min.	Max.	Min.	Max.	
R-Cell Propagation Delays								
t_{RCO}	Sequential Clock to Q		1.00		0.94		1.10	ns
t_{CLR}	Asynchronous Clear to Q		0.66		0.62		0.73	ns
t_{PRESET}	Asynchronous Preset to Q		0.79		0.75		0.88	ns
t_{SUD}	FF Data input setup	0.22		0.21		0.25		ns
t_{SUE}	FF Enable input setup	0.22		0.21		0.25		ns
t_{HD}	FF Data Hold	0.00		0.00		0.00		ns
t_{HE}	FF Enable Hold time	0.00		0.00		0.00		ns
t_{WASYN}	Asynchronous Pulse width	0.48		0.48		0.48		ns
t_{REASYN}	Asynchronous Recovery time	0.00		0.00		0.00		ns
t_{HASYN}	Asynchronous Removal time	0.00		0.00		0.00		ns
t_{CPWHL}	Clock pulse width high to low	0.35		0.35		0.35		ns
t_{CPWLH}	Clock pulse width low to high	0.36		0.36		0.36		ns

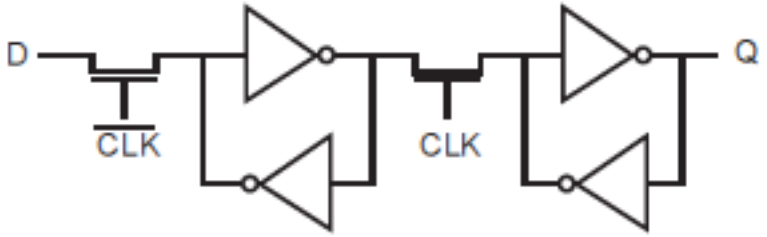


Figure 2-33 • RTAX-S/SL/DSP R-cell Implementation of D Flip-Flop

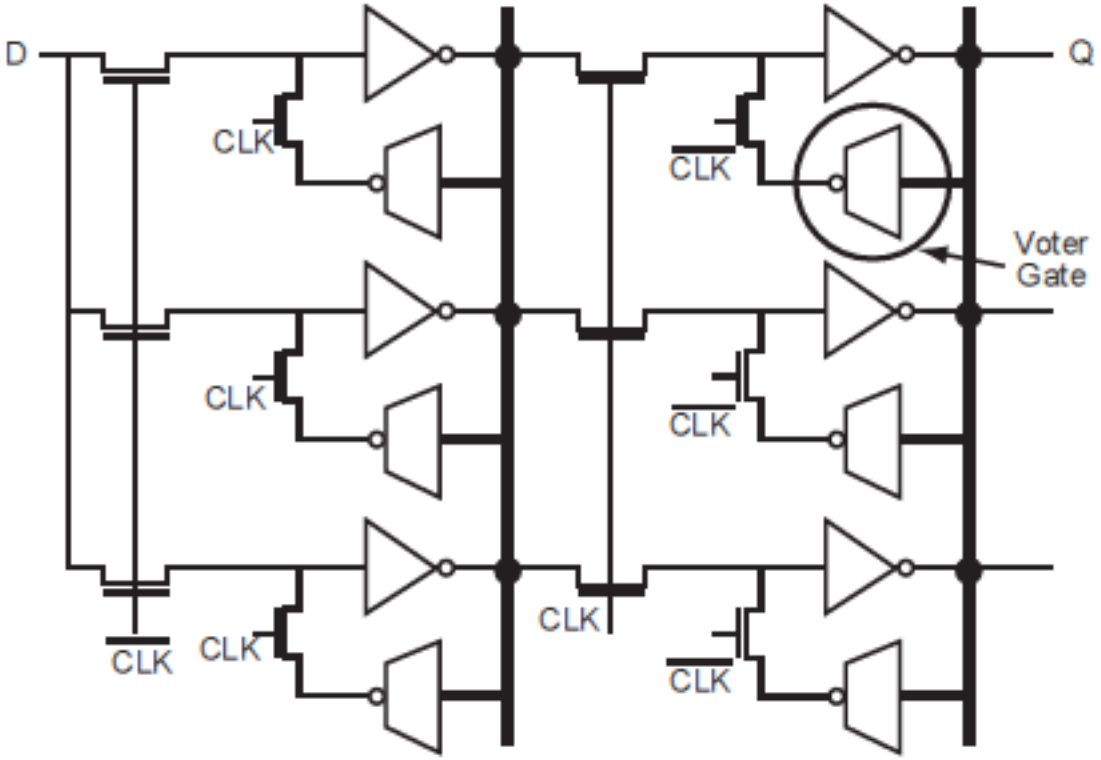
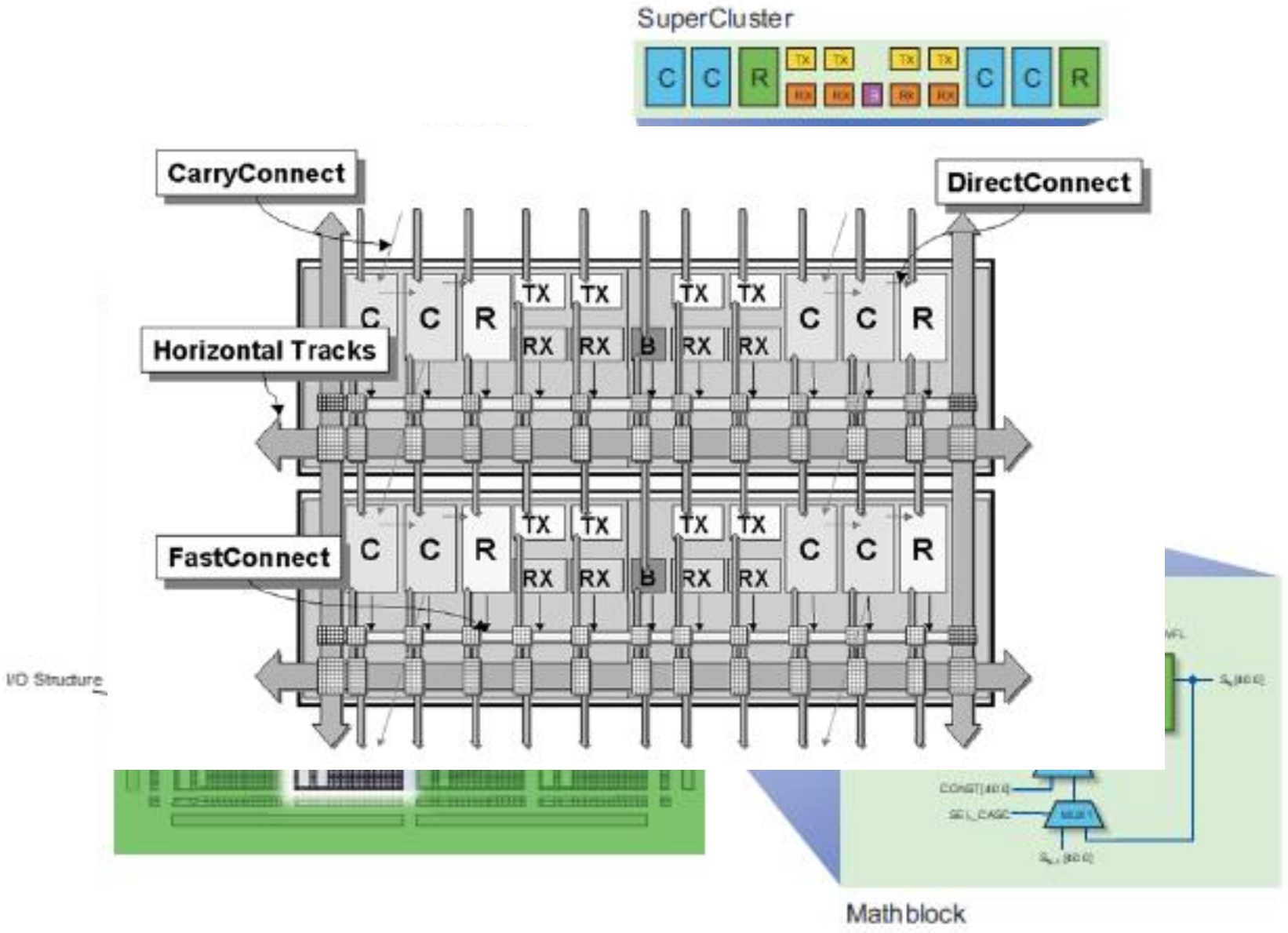
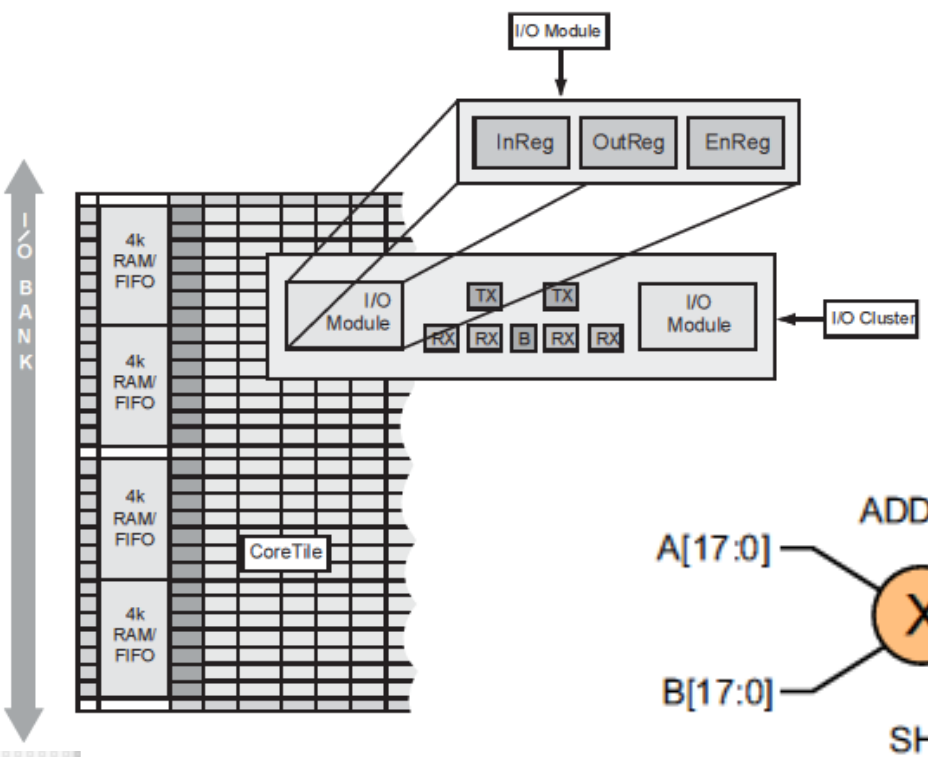


Figure 2-34 • RTAX-S/SL/DSP R-cell Implementation of D Flip-Flop Using Voter Gate Logic


SuperCluster
C
C
R
TX
RX
B
CarryConnect
DirectConnect
Horizontal Tracks
FastConnect
I/O Structure
Mathblock


I/O Module
InReg
OutReg
EnReg
I/O BANK
4k RAM/ FIFO
4k RAM/ FIFO
4k RAM/ FIFO
4k RAM/ FIFO
CoreTile
I/O Module
TX
TX
RX
RX
B
RX
RX
I/O Module
I/O Cluster

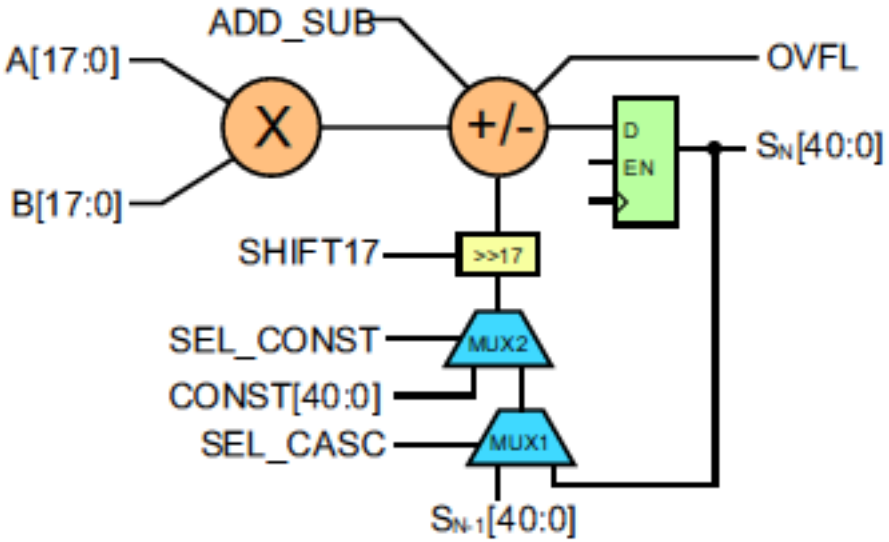

ADD_SUB
A[17:0]
B[17:0]
X
+/-
OVFL
D
EN
SN[40:0]
SHIFT17
>>17
SEL_CONST
MUX2
CONST[40:0]
SEL_CASC
MUX1
SN-1[40:0]

Table 2-8 • **Default Cload / VCCI**

	CLOAD (pF)	VCCI (V)	PLOAD (µW/MHz)	P10 (µW/MHz)	PI/O (µW/MHZ)*
Single-Ended without VREF					
LVCMOS – 15 (JESD8-11)	35	1.5	78.8	49.5	128.3
LVCMOS –18	35	1.8	113.4	73.4	186.8
LVCMOS – 25	35	2.5	218.8	148.0	366.8
LVTTL 8 mA Low Slew	35	3.3	381.2	118.7	499.9
LVTTL 12 mA Low Slew	35	3.3	381.2	138.6	519.8
LVTTL 16 mA Low Slew	35	3.3	381.2	150.8	532.0
LVTTL 24 mA Low Slew	35	3.3	381.2	169.2	550.4
LVTTL 8 mA High Slew	35	3.3	381.2	130.3	511.5
LVTTL 12 mA High Slew	35	3.3	381.2	165.9	547.1
LVTTL 16 mA High Slew	35	3.3	381.2	225.1	606.3
LVTTL 24 mA High Slew	35	3.3	381.2	267.5	648.7
PCI	10	3.3	108.9	218.5	327.4
PCI-X	10	3.3	108.9	162.9	271.8
Single-Ended with VREF					
SSTL2-I	30	2.5	–	171.7	171.7
SSTL2-II	30	2.5	–	148.3	148.3
SSTL3-I	30	3.3	–	327.8	327.8
SSTL3-II	30	3.3	–	288.9	288.9
HSTL-I	20	1.5	–	41.4	41.4
GTLP – 33	10	3.3	–	68.5	68.5
Differential					
LVPECL – 33	N/A	3.3	–	260.6	260.6
LVDS – 25	N/A	2.5	–	145.8	145.8

Note: $*P_{I/O} = P_{10} + C_{load} * VCCI^2$

Otras FPGAs del Mercado

- Lattice
- Atmel
- Aeroflex

Lattice

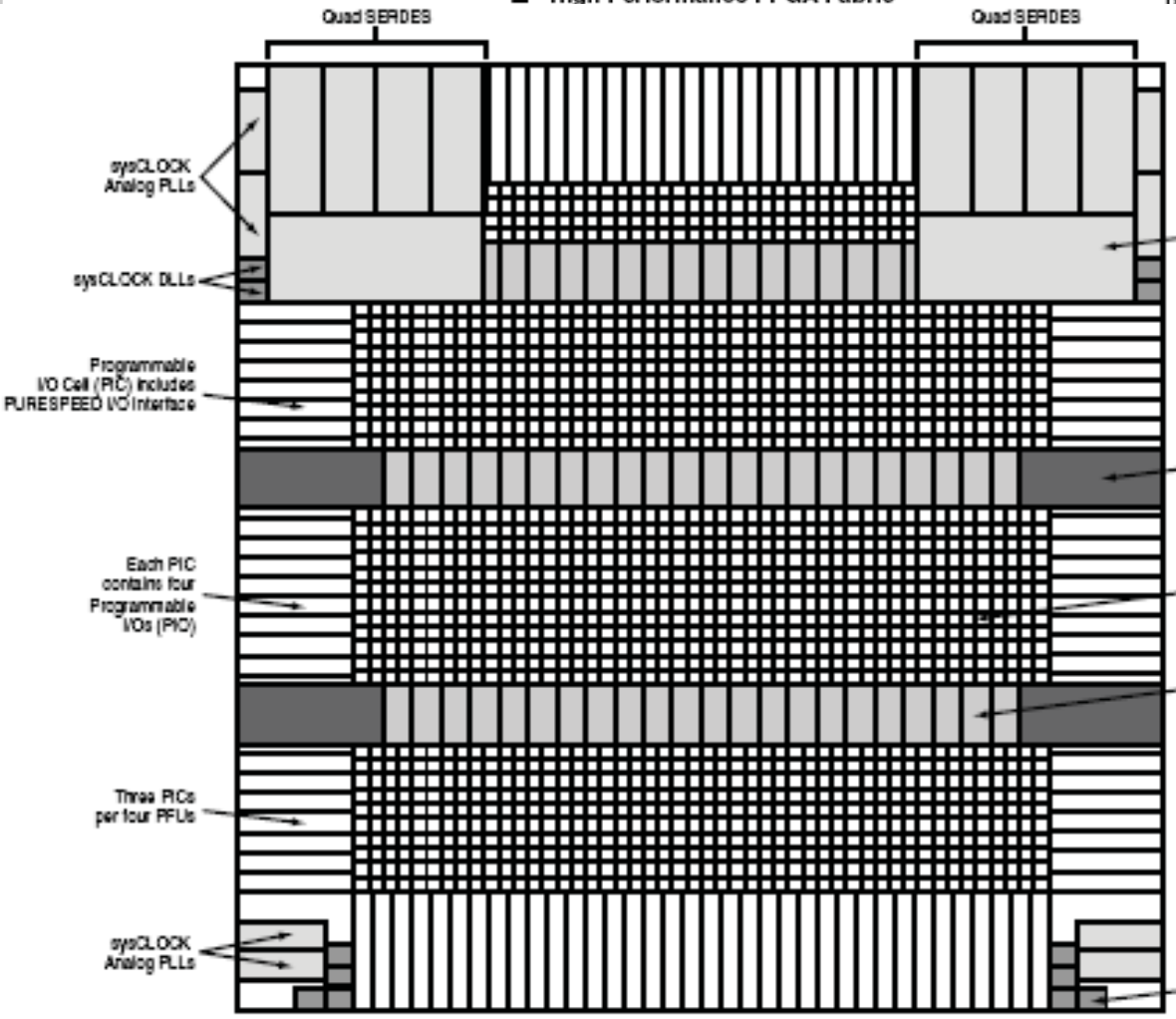
Lattice Semiconductor Corporation

LatticeSC/M Family Data Sheet Introduction

January 2008 — Preliminary Data Sheet DS1004

Features

■ **High Performance FPGA Fabric**



– 1 to 7.8 Mbits memory
– True Dual Port/Pseudo Dual Port/Single

– Includes Thevenin Equivalent and low power V_{TT} termination options

■ **Memory Intensive FPGA**
• sysMEM™ embedded Block RAM

• Embedded PowerPC microprocessor interface
• Low cost wire-bond and high pin count flip-chip packaging
• Low cost SPI Flash RAM configuration

Atmel AT40K y ATF280

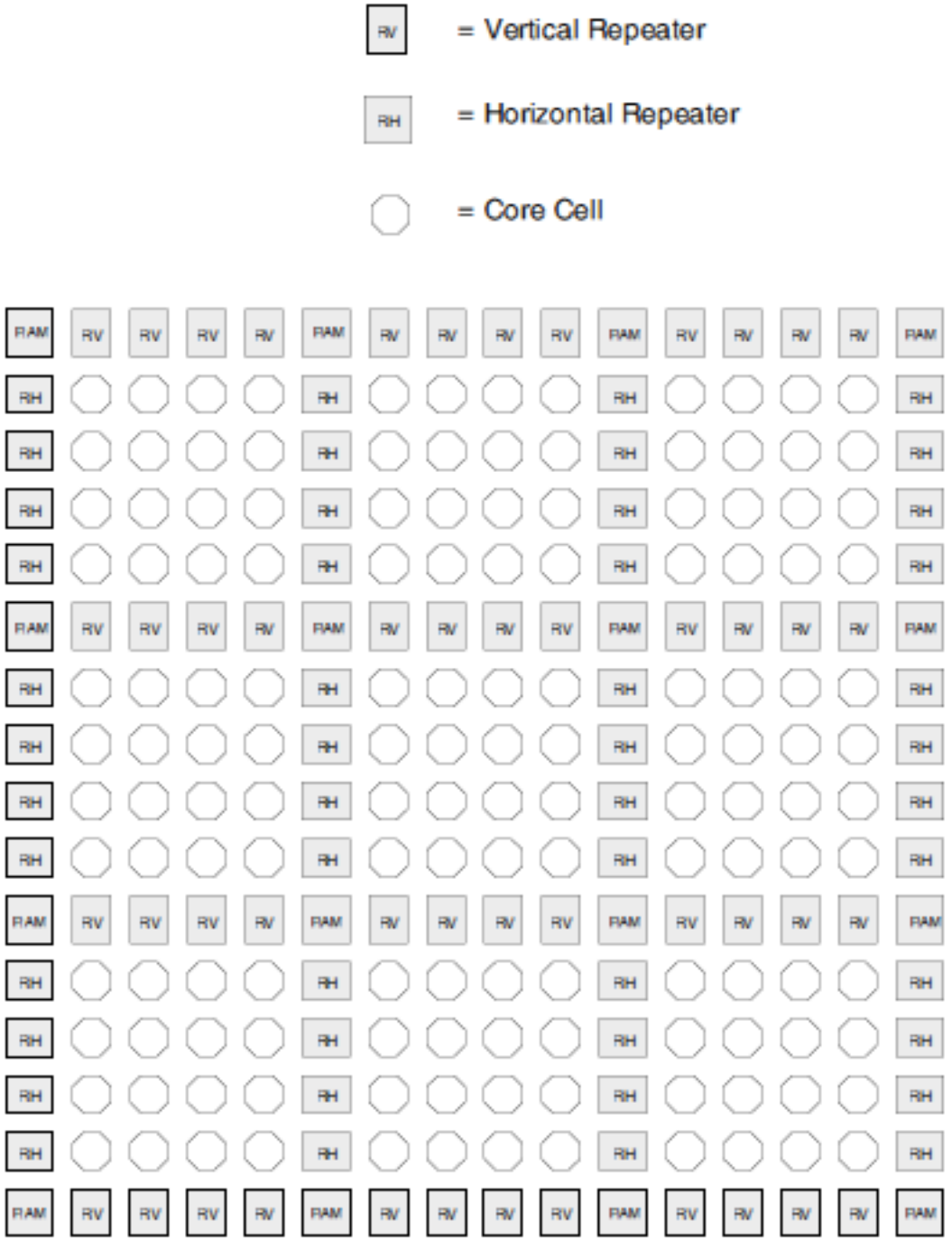
Features

- Ultra High Per
  - System Sp
  - Array Mul
  - 10 ns Flex
  - Internal Ti
- FreeRAM™
  - Flexible, S
  - 2,048 - 18,
- 128 - 384 PCI (
  - Programm
  - Fast, Flex
  - Pin-compa
- 8 Global Clock
  - Fast, Low
  - Programm
  - Distribute
  - Global Re
  - 4 Additior
- Cache Logic®
  - Unlimited
  - Enables A
  - Enables F
  - QuickCha
- Pin-compatibl
  - Plastic Le
  - Thin, Plas
- Industry-stanc
  - Seamless
    Everest, E
    Synplicity
  - Timing Dr
  - Automatic
  - Fast, Effic
  - Over 75 A
    of Reusab
- Easy Migratio
- Supply Voltag
- 5V I/O Toleran
- Green (Pb/Hal

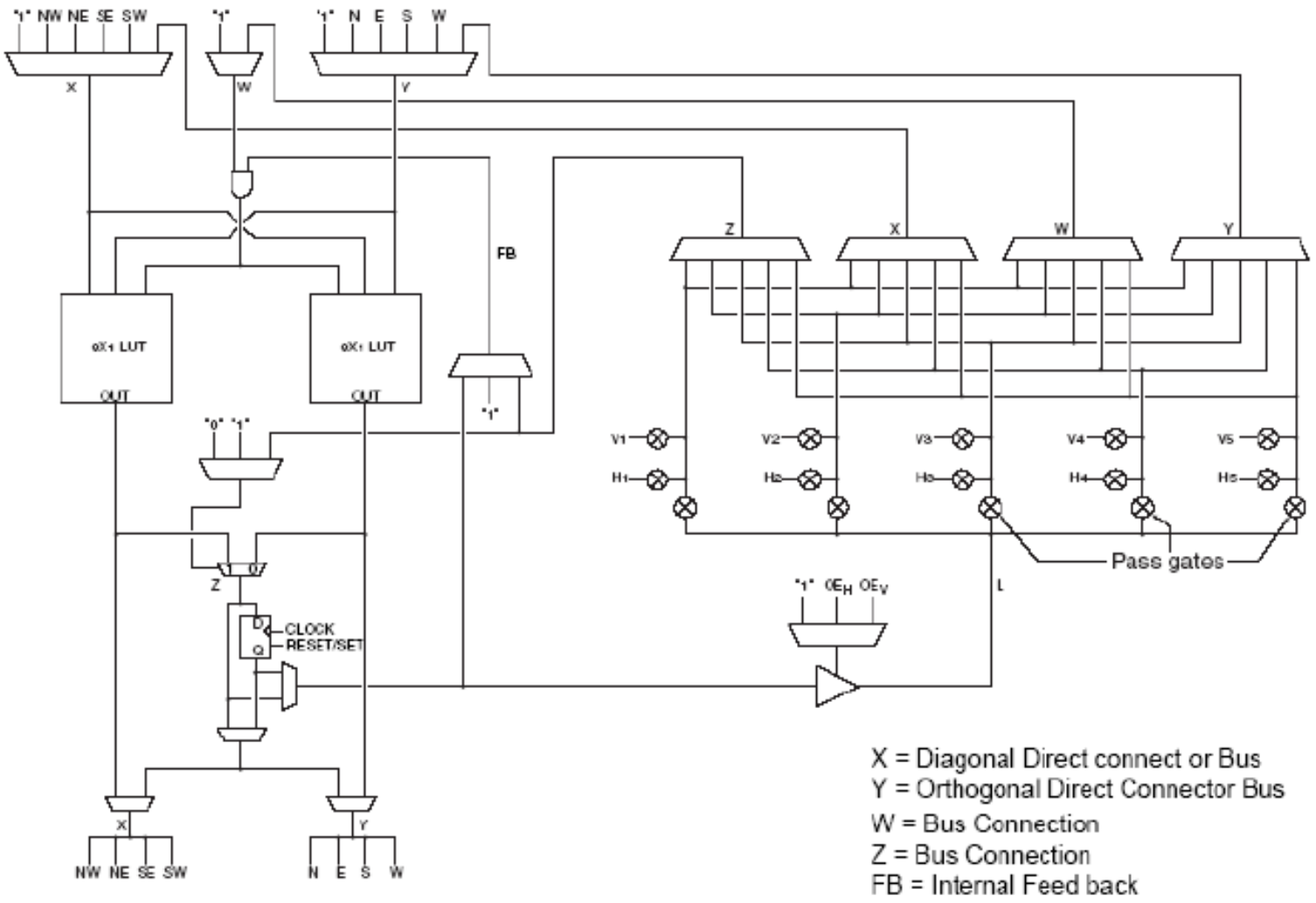
Features

- SRAM based FPGA designed for Space use
  - 280K equivalent ASIC gates
  - Unlimited reprogrammability
  - SEE hardened cells (Configuration RAM, FreeRAM™, DFF, JTAG, I/O buffers)
  - No need for Triple Modular Redundancy (TMR)
- FreeRAM™:
  - 115200 Bits of Distributed RAM
  - 32x4 RAM blocks organization
  - Independent of Logic Cells
  - Single/Dual Port capability
  - Synchronous/Asynchronous capability
- Global Reset Option
- 8 Global Clocks and 4 Fast Clocks
- 8 LVDS transceivers and 8 LVDS receivers
- Cold sparing and PCI Compliant I/Os
  - 308 for 472pins MCGA package
  - 150 for 256pins MQFPF package
- Flexible Configuration modes
  - Master/Slave Capability
  - Serial/Parallel Capability
  - Check of the data during FPGA configuration
- Self Integrity Check (SIC) of the configuration during FPGA operation
- Performance
  - 100 MHz Internal Performance
  - 50MHz System Performance
  - 10ns 32X4 FreeRAM™ access time
- Operating range
  - Voltages
    - 1.65V to 1.95V (Core)
    - 3V to 3.6V (Clustered I/Os)
  - Temperature
    - - 55°C to +125°C
- Radiation Performance
  - Total Dose tested up to 300 krads (Si)
  - No single event latch-up below a LET of 80 MeV/mg/cm2
- ESD better than 2000V
- Quality Grades
  - QML-Q or V
  - ESCC
- Ceramic packages
  - 256pins MQFPF (150 I/Os, 8 LVDS Tx and 8 LVDS Rx)
  - 472pins MCGA (308 I/Os, 8 LVDS Tx and 8 LVDS Rx)
- Design Kit including
  - ATF280E and Configurator Samples
  - Evaluation Board
  - Software Design Tools
  - ISP Cable/Dongle

Arquitectura



Célula básica de ATMEL

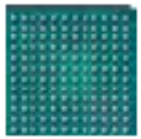


FG896

f IGLOOe[1]
ProASIC3E[1]
ProASIC3L[1]
Military ProASIC3/EL[1]
ps 31x31 mm
h 2.23 mm
p 1.00 mm

FG144

f IGLOO[1]
ProASIC3[1]
ProASIC3L[1]
Military ProASIC3/EL[1]
ps 13x13 mm
h 1.45 mm
p 1.00 mm



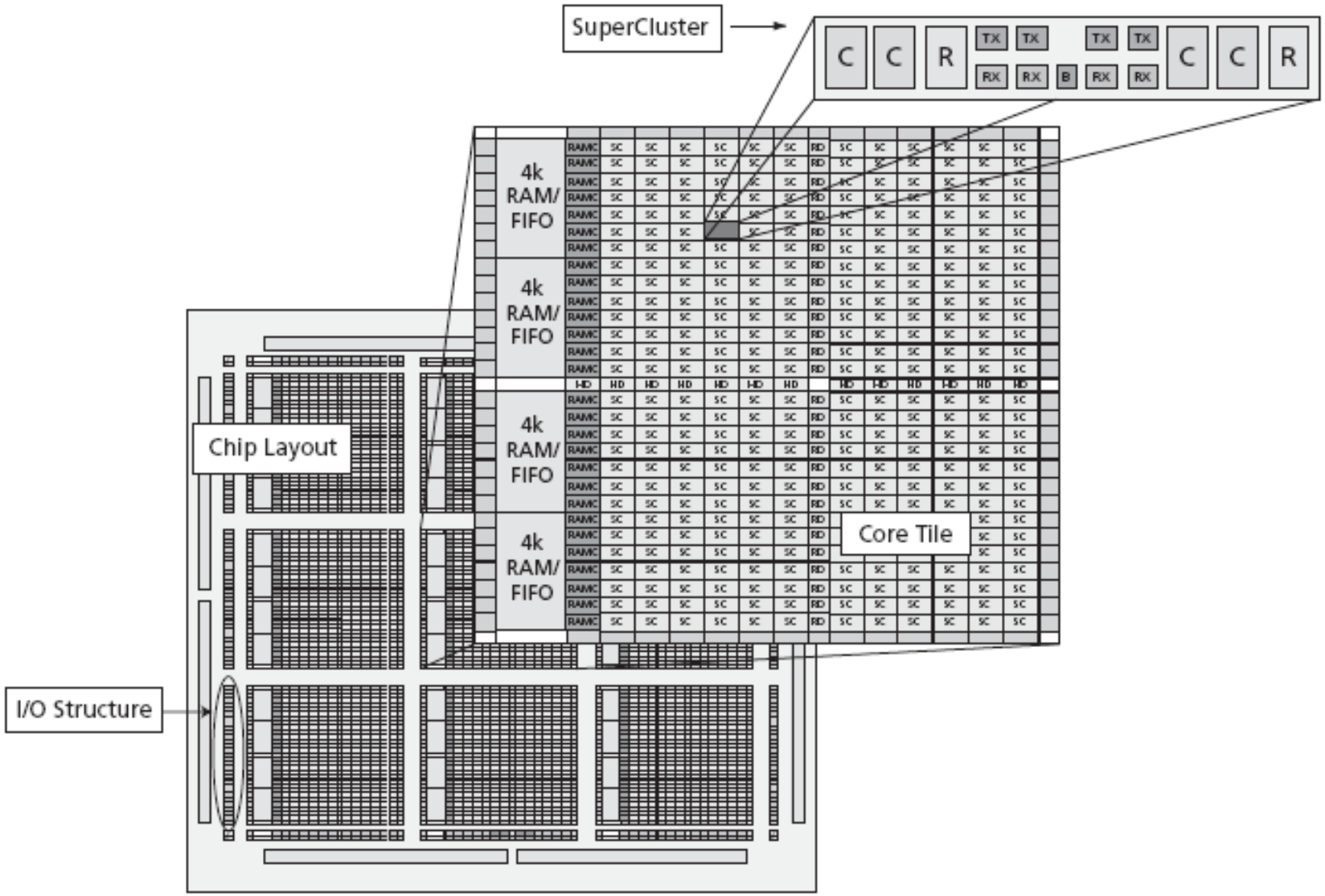
CQ352

f Military ProASIC[PLUS]
ps 48x48 mm
h 2.67 mm
p 0.50 mm

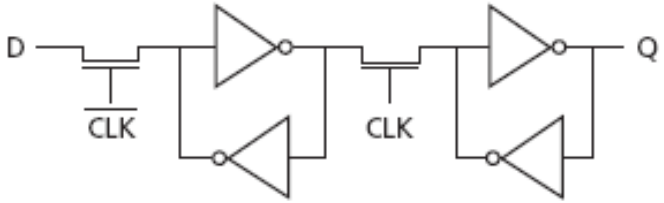
Apéndice A. Efectos de la Radiactividad. FPGA Microsemi RTAX

- Inmunidad a SEUs por radiación: LET_{th}>37 MeVcm^2/mg
- SEU Rate 10^{-10} Errores / Bit-Day
- Protección a SRAM interna mediante EDAC para SEU doble
- Inmunidad a SELs por radiación: LET_{th}>104 MeVcm^2/mg
- Dosis Máxima: 300 Krad
- Puertas Equivalentes: 250K a 2M
- Número de Flip-flops alta inmunidad: 10752
- Hasta 288Kbits
- Tecnología antifusible, 0.15μm y 7 capas de metal

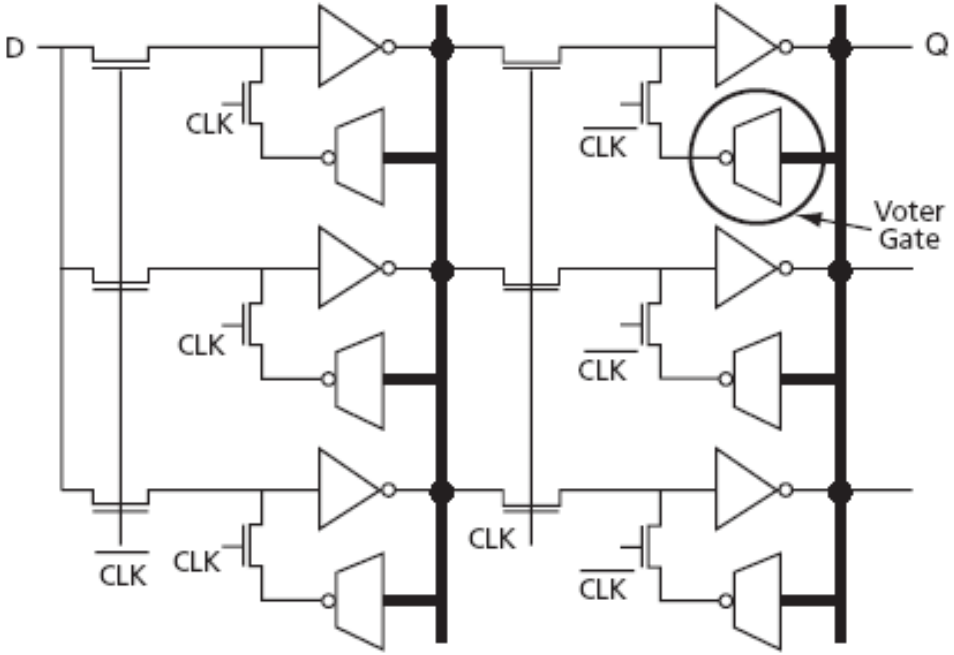
Arquitectura de la serie RTAX



Flip-flop con inmunidad



RTAX-S R-cell Implementation of D Flip-Flop



RTAX-S R-cell Implementation of D Flip-Flop Using Voter Gate Logic

Apéndice: FPGAs para aplicaciones aeroespaciales. Propuesta de Xilinx

- Dosis total 200 Krad
- Inmunidad a Latchup: LET_{th}> 160MeV cm^2/mg
- Inmunidad a SEU $1.5*10^{-6}$ SEU/bit día
- Arquitectura comercial, equivalente a Virtex II.
- Soporta hasta la XC2V6000 (6M)
- Necesita herramientas para protección por diseño como XTMRtool

Especificaciones de radiación

Radiation Specifications(1)

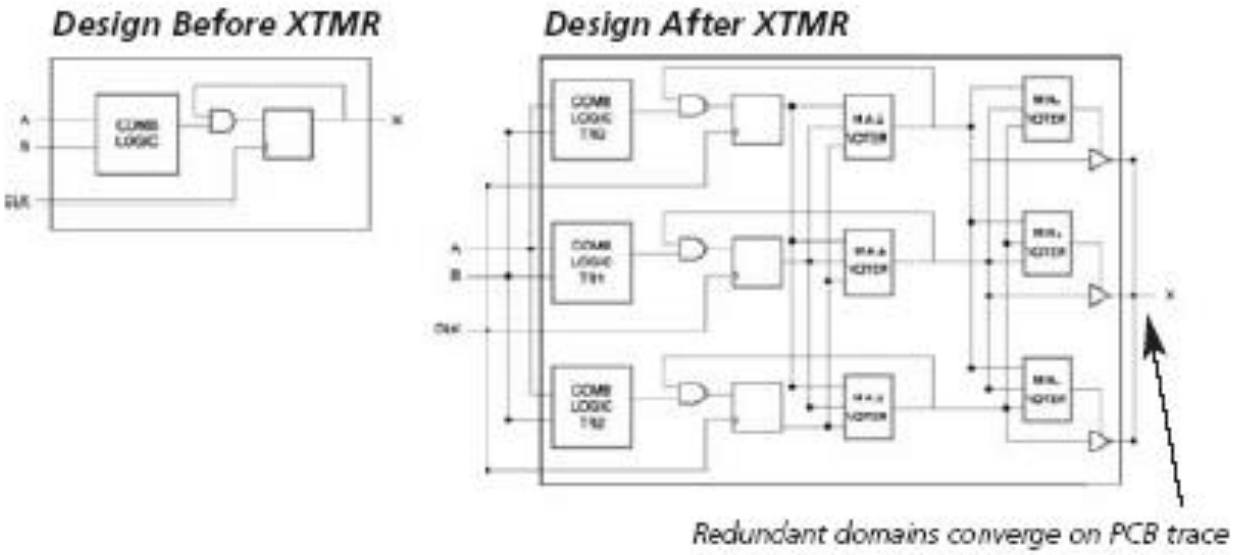
Table 3: **Minimum Radiation Tolerances**

Symbol	Description	Min	Max	Units
TID	Total Ionizing Dose Method 1019.5, Dose Rate ~50.0 rad(Si)/sec	200	-	krad(Si)
SEL	Single Event Latch-up Immunity Heavy Ion Linear Energy Transfer (LET)	160	-	(MeV-cm^2/mg)
SEFI	Single Event Functional Interrupt GEO 36,000km Typical Day		1.5E-6	Upsets/Device/ Day

Notes:

1. For more information, refer to "Single Event Effects Consortium Report, Static SEU Response for the Rad Hard Virtex-II" at http://www.xilinx.com/products/hirel_qml.htm.

XTMRtool



No es suficiente con redundar la lógica. Se necesita más acción:

- Scrubbing
- Placement

FEATURES

- 0.25µm, five-layer metal, ViaLink™ epitaxial CMOS process for smallest die sizes
- One-time programmable, ViaLink technology for personalization
- Typical performance characteristics -- 120 MHz 16-bit counters, 120 MHz datapaths, 60+ MHz FIFOs
- 2.5V core supply voltage, 3.3V I/O supply voltage
- Up to 320,000 system gates (non-volatile)
- I/Os
  - Interfaces with 3.3 volt
  - PCI compliant with 3.3 volt
  - Full JTAG 1149.1 compliant
  - Registered I/O cells with individually controlled enables
- Radiation-hardened design; total dose irradiation testing to MIL-STD-883 Test Method 1019
  - Total-dose: 300 krad(Si)
  - SEL Immune: >120MeV-cm^2/mg
  - LET_{TH} (0.25) MeV-cm^2/mg:
    >42 logic cell flip flops
    >64 for embedded SRAM
  - Saturated Cross Section (cm2) per bit
    5.0E-7 logic cell flip flops
    2.0E-7 embedded SRAM
- Up to 24 dual-port RadHard SRAM modules, organized in user-configurable 2,304 bit blocks
  - 5ns access times, each port independently accessible
  - Fast and efficient for FIFO, RAM, and initialized RAM functions
- 100% routable with full logic cell utilization and 100% user fixed I/O
- Variable-grain logic cells provide high performance and 100% utilization
- Typical logic utilization = 65-80% (design dependent)
- Comprehensive design tools include high quality Verilog/ VHDL synthesis and simulation
- QuickLogic IP available for microcontrollers, DRAM controllers, USART and PCI
- Packaged in a 208-pin CQFP, 288 CQFP, 484 CCGA, 484 CLGA, 208 PQFP, 280 PBGA, and 484 PBGA
- Standard Microcircuit Drawing 5962-04229
  - QML qualified

eroflex

INTRODUCTION

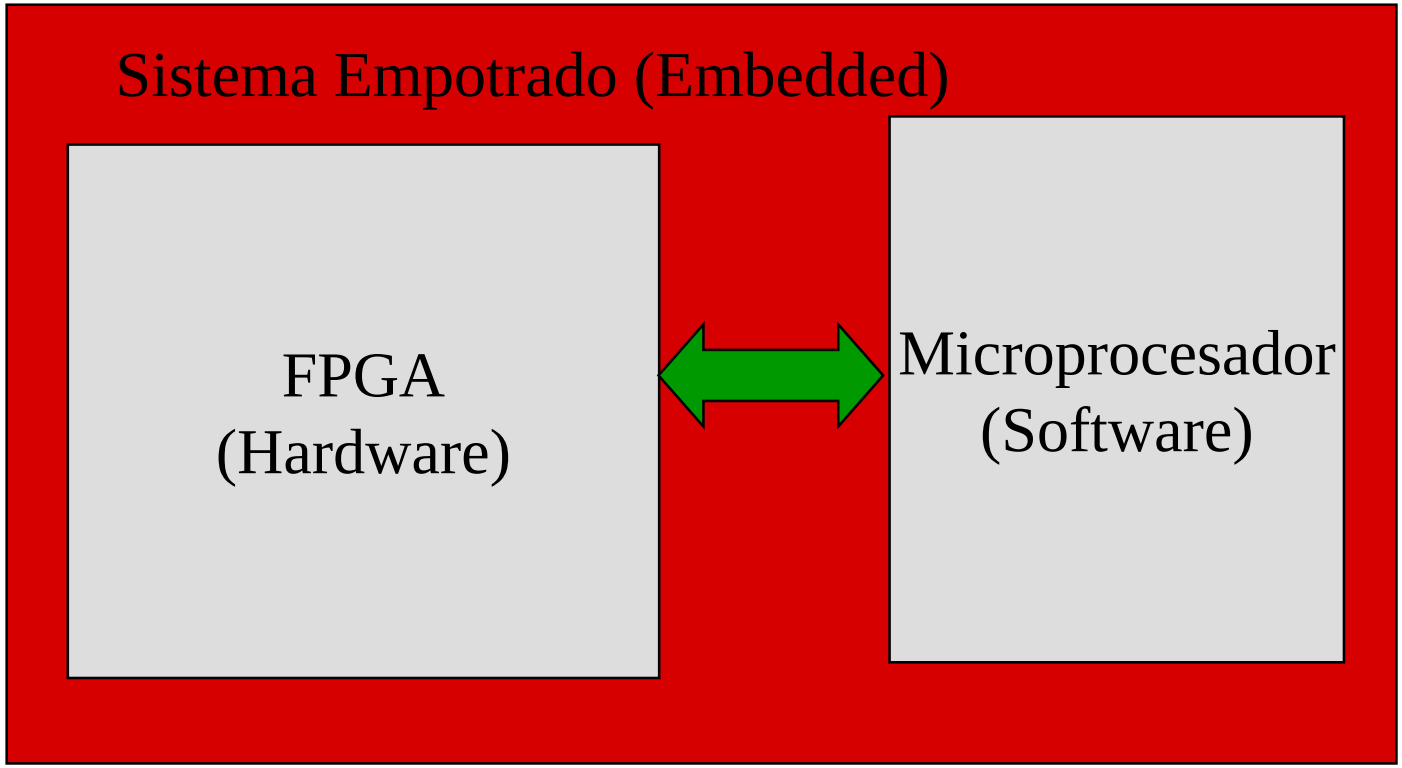
The RadHard Eclipse Field Programmable Gate Array Family (FPGA) offers up to 320,000 system gates including Dual-Port RadHard SRAM modules. It is fabricated on 0.25µm five-layer metal ViaLink CMOS process and contains 1,536 logic cells and 24 dual-port RadHard SRAM modules (see Figure 1 Block Diagram). Each SRAM module has 2,304 RAM bits, for a maximum total of 55,300 bits. Please reference product family features chart on page 2.

SRAM modules are Dual Port (one asynchronous/synchronous read port, one write port) and can be configured into one of four modes (see Figure 2). Designers can cascade multiple RAM modules to increase the depth or width allowed in single modules by connecting corresponding address lines together and dividing the words between modules (see Figure 3). This approach allows a variety of address depths and word widths to be tailored to a specific application.

The RadHard Eclipse FPGA is available in a 208-pin Cerquad Flatpack, allowing access to 99 bidirectional signal I/O, 1 dedicated clock, 8 programmable clocks and 16 high drive inputs. Other package options include a 288 CQFP, 484 CCGA and a 484 CLGA.

Aeroflex uses QuickLogic Corporation's licensed ESP (Embedded Standard Products) technology. QuickLogic is a pioneer in the FPGA semiconductor and software tools field.

Apéndice B: Sistemas empotrados



Sistemas Hardware:
- Rápidos
- Eficientes
- Paralelos
- Ad hoc

Sistemas Software
- Fáciles
- Decisiones
- Serie
- Propósito General

Propuesta de Xilinx

- Virtex II Pro:
  - 1 ó 2 IBM PowerPC 405 diseñados en silicio
- El resto, uso de "soft cores" de microprocesadores:
  - MicroBlaze
  - PicoBlaze

Propuesta de ALTERA

- Excalibur
  - ARM7
- El resto, uso de “soft cores” de microprocesadores:
  - NIOS

Propuesta de ACTEL

- Uso del ARM7